

CMOS CURRENT-MODE INTEGRATOR AND DIFFERENTIATOR FOR LOW VOLTAGE AND LOW POWER APPLICATIONS

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ABSTRACT

A new approach for CMOS Current-Mode Integrator (CMI) and Differentiator (CMD) realization are presented in this work. The proposed circuits are employed the inverter-based second-generation current conveyor (CCII). The CCII circuit achieves minimum number of stack transistors between the rail supply and class AB operation ability. Therefore, the proposed circuits are considered as low voltage and low power (LVLP) analog circuit. Moreover, the programmability of the proposed CMI and CMD can be realized using transconductance gain of the CMOS inverter. The CMOS inverter is characterized using a set of free hand equations, which are modeled the CMOS inverter as analog device. The high input impedance of the CMOS inverter simplifies design of the op-amp since it is loaded only by capacitor. Second order filter is realized using the proposed CMI and CMD. The designed filter achieved independently center frequency (ω_0) and quality factor (Q) tuning. The proposed circuits are designed and simulated using the MOST parameters of IBM 0.13 μ CMOS technology.

Keywords: CMOS analog circuit design, Current mode integrator (CMI), Current mode signal processing, current conveyor (CCII), current mode differentiator (CMD), low voltage low power (LVLP), and Biquad filter.

1. Introduction

Recently, the research in analog integrated circuits has been become in the direction of low voltage (LV) and low power (LP) design due to market requirements and the technologies constrain. The environment of portable systems is most requirements in side of market. Also, the dramatically growth of submicron technology has been forced the researchers to work at low voltage supply. These LV circuits have to show a reduction of power consumption to maintain a longer battery lifetime. In this area, the obstacles of the voltage-mode signal processing techniques such as the gain-bandwidth product limitation, dynamic range, ...etc, are going to be overcome by the current-mode approaches [1,2,3]. The current mode circuits are used as low voltage due to, the current signal is compressed as voltage mode using active devices. The current-conveyor [4, 5] has been considered as basic circuit block of the current-mode architectures, because all the active devices (amplifier, integrator, differentiator, ...etc) can be made of a suitable connection of one or two CCII's. Moreover, for the CCII becomes attractive in portable systems, then LV and LP ability have to achieve. In low voltage current mode technique such the switched-MOSFET [6, 7], the memory MOST is worked in triode region which, represent as resistive load to the amplifier. Therefore, the amplifier must be able to drive the required load current, which is making the opamp as source of power consumption.

Finally, the current-mode integrator is an important circuit block, which is widely used in analog signal processing applications, such as, filter design, waveform shaping,

process controller design, calibration circuits, ...etc. Recently, there is a strong direction for a resistance less and capacitor less circuit design such in [8, 9]. Therefore, the analog circuit has been focused on the active only analog circuit implementation. The OTA structure has been used as active only circuit realization [8]. This technique is not suitable for low voltage and low power circuit design since it has been constructed using three transconductance sections and operation amplifier as shown in Fig. 1. Also, this approach has employed the compensation capacitor of the op-amp (A_1) as integrator capacitor.

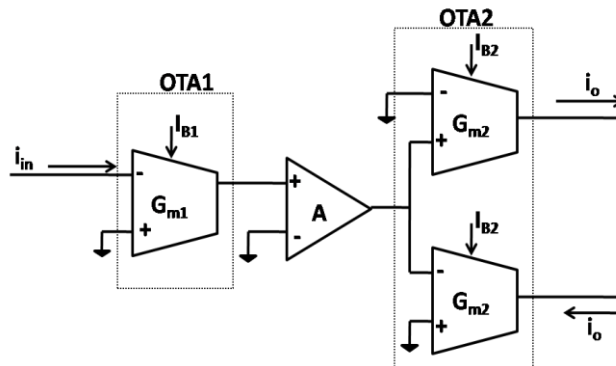


Fig. 1. Active only current mode integrator proposed in [8].

In this paper, the current-mode integrator (CMI) and differentiator (CMD) circuits are presented. This article is organized as following: For concept revision, the CMOS inverter based Current Mirror (CM) and Current conveyor circuit, are mentioned in section I. The basic element of this work (CMOS inverter) is analyzed and set of design equations are developed in section II. The new topologies of current-mode integrator and differentiator are proposed and analyzed in section III. The simulation and verification of the designed circuits are illustrated in paragraph IV. The current mode second order filter and its programmability are in section V. Finally, conclusion is presented in section VI.

2. CMOS Inverter Based Current Mirror

Recently, the CMOS inverter has been employed as LVLP analog transconductance block [10, 11]. In the conventional Current Mirror (CM) shown in Fig. 2(a), transistor (M_2) must work in saturation to obtain the mirroring function. The class AB current mirror [12,13] is realized as two complementary MOS current mirrors as shown in Fig. 2(b). The proposed cell has low-power dissipation characteristic and it provides up and down mirrored current. In the circuit shown in Fig. 2(b), the input and output voltages (V_{in} & V_o) may be selected as DC level and it must be chosen to preserve the symmetric characteristic in terms of the input current. As shown in Fig. 2(b), the output current equals input current as long as the two CMOS inverters are matched and V_x is equal to V_y . Therefore, the cell in Fig.2(c) is more accurate with respect to that in Fig.2 (b).

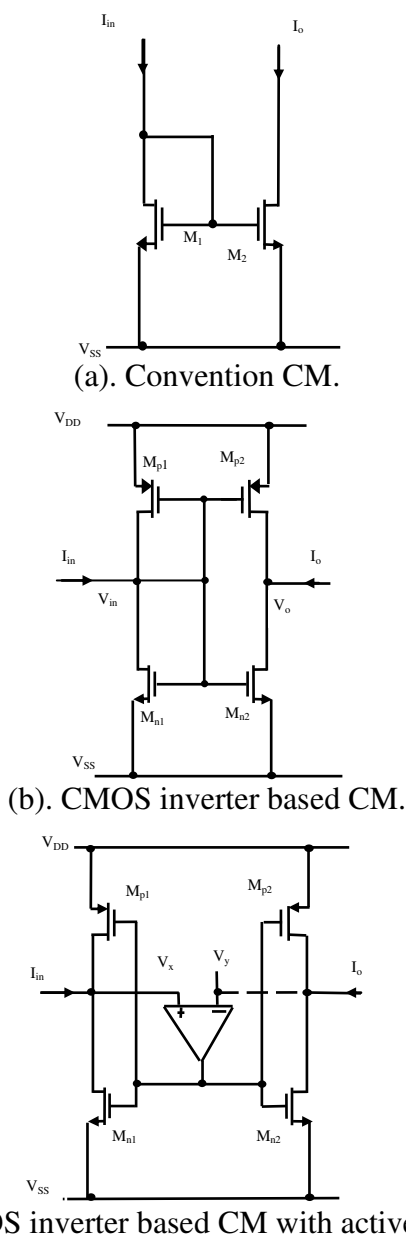
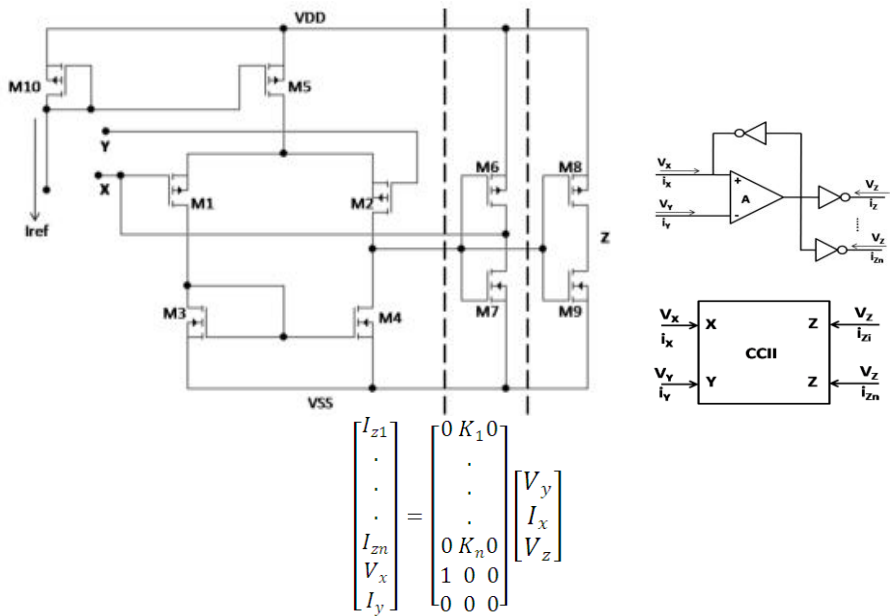


Fig. 2.Convention and class AB current mirrors [12].

Moreover, a low voltage and low power CCII inverter based has been published [12,13]. The basic cell is illustrated in Fig. 3. The input current is translated as voltage (compressed signal) in the internal output of the first stage (V_{DS} of M_4). The transfer function is square root relation (in saturation). In Fig. 3, the input current into low input impedance terminal "x" will be conveyed to z-terminal if and only if, M_6 and M_8 , also, M_7 and M_9 are

identically. There is no load to the amplifier except the parasitic capacitors ($C_{gsn}+C_{gsp}$), which means low power consumption at very high frequency applications. This CCII approach has been achieved high accuracy current conveyor ratio (i_z/i_x) since the current error is function of open loop gain of the Op-Amp [14]. The output impedance causes a current error which has been cancelled with the operating condition ($V_x=V_y=V_z=V_m$). Where, V_m is DC level voltage. Fig.3(b) shows the simplicity of getting out a copies of I_x ($I_{z1}, I_{z2}, \dots, I_{zn}$). K_1, K_2, \dots and K_n are current gains at ports z_1, z_2, \dots and z_n , respectively. The K_n is number of CMOS inverters connected in parallel. All output ports are virtually equal V_z .



(a). The CCII circuit schematic. (b). The CCII symbol and Ch/s.

Fig. 3. The basic CCII cell proposed in [12, 13].

3. CMOS Inverter Analysis

The conventional CMOS inverter shown in Fig. 4(a) works as analog block since it works at V_m and I_o operating point. V_m is input voltage, which achieved output voltage equal V_m , and I_o is draining current of M_n and M_p ($I_{dsn} = I_{dsp}$). The CMOS inverter is considered as transconductance circuit especially at output voltage equal V_m . The rail-to-rail output ability and class AB operation are originally characteristic of the CMOS inverter as depicted in Fig. 4(b). This section proposes a methodology for trade off between the sizes of both M_n and M_p transistors to the DC operating point (V_m, I_o). The proposed design approach is based on the ACM model [15], which is dedicated for analog circuit design. In Fig. 4, assume all transistors in saturation, the quiescent point (V_m, I_o) can be calculated as :

$$V_m = \frac{V_{DD} - V_{tp} + V_{tn} \sqrt{\frac{i_{fpo}}{i_{fno}}}}{1 + \sqrt{\frac{i_{fpo}}{i_{fno}}}} \quad (1)$$

And

$$I_o = \frac{\mu_n * C'_{ox} * \left(\frac{W}{L}\right)_n}{2 * n_n} \left(\frac{V_{DD} - V_{tp} + V_{tn} \sqrt{\frac{i_{fpo}}{i_{fno}}}}{1 + \sqrt{\frac{i_{fpo}}{i_{fno}}}} - V_{tn} \right)^2 \quad (2)$$

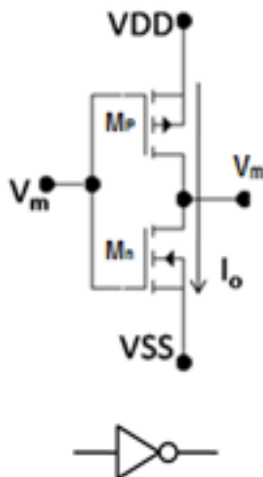
Where, $I_o = I_{dsn} = I_{dsp}$ ($I_{out} = 0$), and $V_o = V_m$. i_{fpo} and i_{fno} are the inversion levels of M_n and M_p , respectively. V_{tn} and V_{tp} are the threshold voltage of M_n and M_p , respectively. Generally, i_f is the normalized drain current or inversion level [15,16], which is defined as;

$$i_f = \frac{I_D}{I_S} \quad (3)$$

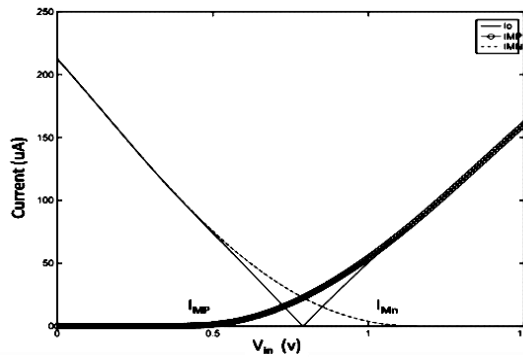
and

$$I_S = \mu_n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \quad (4)$$

Where, I_S , the normalization current, mobility μ , oxide capacitance per unit area C'_{ox} and the thermal voltage ϕ_t . n , the slope factor, is slightly greater than one.



(a). CMOS inverter and its symbol.



(b).Its I-V Characteristic .

Fig. 4.Conventional CMOS inverter.

Moreover, the bandwidth of the transconductance cell is limited by the all attached parasitic capacitors to the output node ($C_L \cong C_{gdn} + C_{gdp}$). The low frequency gain (A_V), the unity gain bandwidth (GB) expression, and the output impedance (r_o) can be approximated as;

$$A_V = (g_{mn} + g_{mp})r_o \quad \text{and} \quad GB = (g_{mn} + g_{mp})/C_L \quad (5)$$

Where, $g_{mn(p)}$ is transconductance of $M_{n(p)}$, respectively, which can be calculates as;

$$\frac{g_{mn(p)}}{I_o} = \frac{(2/\phi_t)n}{1 + \sqrt{1 + i_{fn(p)}}} \quad (6)$$

And $r_o = (r_{dsn}/r_{dsp})$. Eq.'s 1 to 6; are used for pre-design of the CMOS inverter. The design methodology steps can be summarized as:

1. The operating voltage (V_m biased voltage) is selected to avoid the conduction gap problem [17] due to MOST threshold voltage at low supply voltage.
2. The ratio between i_{fpo}/i_{fno} can be defined, Eq. 1.
3. From power consumption (I_o), the M_n transistor size $(W/L)_n$ has been defined, Eq. 2.
4. The frequency response (GB) of the designed CMOS inverter can be tested.

Just to verify this analysis, the comparison between the analysis and simulator result are shown in Fig. 5. The variation between the operating point (V_m, I_o) versus the MOS transistors (n and p channel) size ratio $\{K_r = (\mu W/L)_n / (\mu W/L)_p\}$ indicates that the curves are very closing.

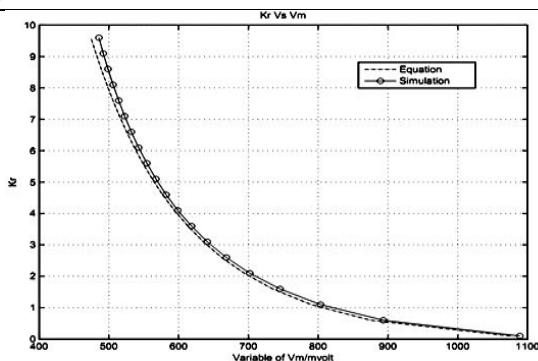


Fig. 5. The operating point voltage (V_m) varies the $K_r\{i_{fpo}/i_{fno}\}$.

4. Proposed CCII Integrator and Differentiator

In this section, new topologies of the CMOS current-mode integrator (CMI) and differentiator (CMD) are proposed. In this circuit, the current conveys to output terminal with integrated/differentiated relation. The proposed circuits are based on the second generation current conveyor circuit (CCII) published in [12,13]. First, the proposed current-mode integrator is shown in Fig.6. In this circuit, the input signal is processed as:

1. The input current (I_x) is integrated into the feedback capacitor, which generates an output voltage (V_{DS} of M_7), lagging by 90° phase shift with respect to the input current.
2. The generated voltage is used to obtain the output current using the CMOS inverter (M_8 and M_9) as transconductance "OTA" cell.
3. All terminal voltages (V_x , V_y , and V_z) are constant and equal DC value (biasing voltage $V_y = V_m$).

The biased voltage is generated using the diode connection configuration of the CMOS inverter (input shorted to output terminal at no drawn output current).

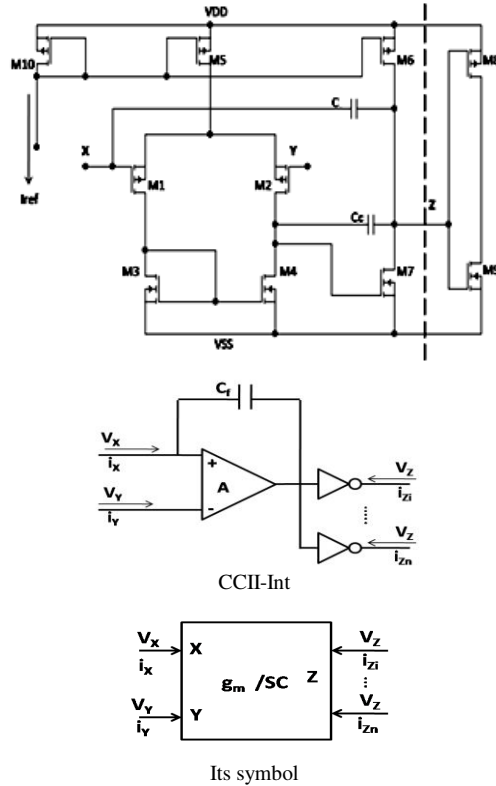


Fig. 6. The proposed second-generation current conveyor integrator (CMI).

Ideally, the characteristic of current-mode integrator shown in Fig. 6, can be summarized in the following equation.

$$\begin{bmatrix} I_z \\ V_x \\ I_y \end{bmatrix} = \begin{bmatrix} 0 & -\frac{g_m}{SC} & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{7}$$

Eq. 7, provides highly wide band frequency integrated range. In practical, the dominant pole eliminates the low frequency applications of a real integrator as shown in Eq. 8. In ultra low frequency applications such biomedical [18], very large capacitor is employed for pole location very closely to zero frequency. Therefore, passive large capacitor "out of chip" must be used, or active large capacitor has been employed [19]. For this reason, the small signal analysis of the proposed CMI is done. The real current transfer function i_z/i_x is approximated as;

$$\frac{i_z}{i_x} \cong \frac{-g_m A_v r_o}{1 + A_v r_o C s} \tag{8}$$

Where A_v is op-amp open loop gain, r_o is output resistance of CMOS inverter, and g_m is transconductance of the CMOS inverter. Equation 8, is consider ideal integrator (Eq. 7)

when, either large miller capacitor, or high output impedance, or very high gain amplifier is used. For this reason, the op-amp is designed as two stages amplifier to achieve high gain.

Moreover, the Current-Mode Differentiator (CMD) is realized using the same strategy as shown in Fig. 7. The proposed CCII differentiator is characterized as:

$$\begin{bmatrix} I_z \\ V_x \\ I_y \end{bmatrix} = \begin{bmatrix} 0 & -\frac{S.C}{g_m} & 0 \\ g_m & 100 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (9)$$

In this circuit topology; the current error is minimized at the terminal voltages are equal to V_m ($V_x=V_y=V_z$).

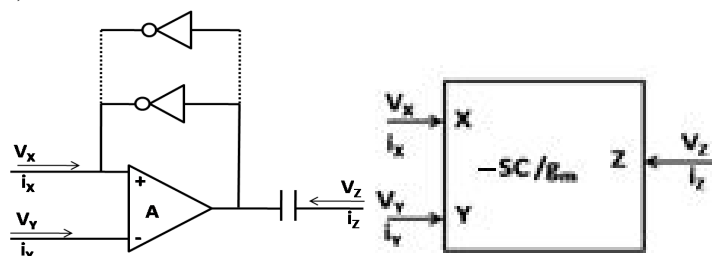


Fig.7. The proposed CMD and its symbol.

5. Verification and Simulation

The proposed CCII integrator and differentiator are designed to fabricate in IBM 0.13 μ CMOS technology from MOSIS. A two stages operational amplifier shown in Fig. 6, has been designed for 80dB open loop gain, 100MHz unity gain bandwidth, and 56 $^\circ$ phase shift. The strategy in [20] is employed for circuit design. The design results are in table I. Also, the CMOS transconductance has been designed using the results in section II. The CMOS inverter is designed with high output impedance (r_o) to satisfy an approximately ideal current source. So, both of N- and P- MOST length (L) should be high enough. The CMOS inverter parameters and transistors size are shown in table II. The CCII integrator and differentiator are realized using 2pF feedback capacitor.

Table1.

OP-AMP TRANSISTORS SIZE.

Transistor	W(μ)	L(μ)
M ₁ , M ₂	100	1
M ₃ , M ₄	5	1
M ₅ , M ₈	30	1
M ₆	150	1
M ₇	450	1
C _L	4pF	
C _C	1pF	
I _{ref}	95 μ A	

Table 2.
CMOS Inverter CH/s

Parameter	Value
$W_{n/p}(\mu)$	2/4
$L_{n/p}(\mu)$	5/5
$V_m(\text{mV})$	655
$I_o(\mu\text{A})$	24
$g_m(\mu\text{S})$	147
$r_o(\text{M}\Omega)$	4.65

Fig. 8, depicts the time response of the proposed current mode integrator which shows the good integration relation between the input and the conveyed current.

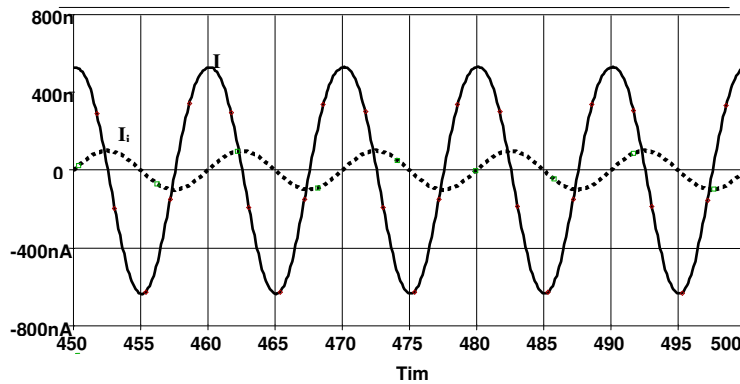


Fig. 8. Input to output current relation of the proposed CMI.

We emphasize that, in this CCII circuits topology, v_x, v_y and v_z must be constant and equal to V_m for good results. In addition, the frequency responses of the proposed (integrator/differentiator) circuits are tested as shown in Fig. 9. The simulation illustrates the proposed CMI and CMD frequency range is very wide (1Hz - 6×10^6 Hz) with $\pm 5^\circ$ maximum phase error.

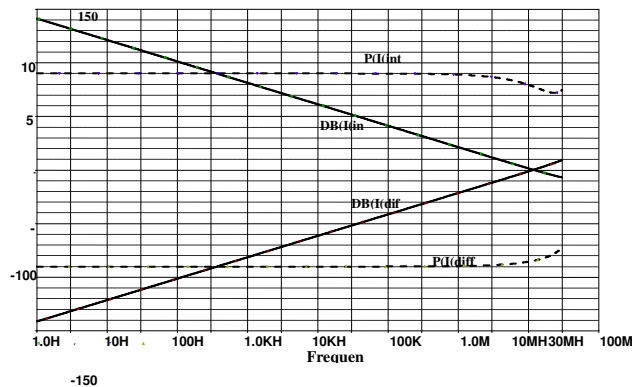


Fig. 9. Frequency response of the proposed CCII integrator and differentiator.

6. Current-Mode Second Order Filter

Fig.10 shows the block diagram of the tunable current-mode filter based on the proposed CCII integrator, differentiator and the CMOS inverter- based current conveyor circuit (CCII) [12,14]. Low pass, band pass and high pass output currents "I_{LP}, I_{BP}, and I_{HP}", respectively, are related to the input current as follow:

$$\frac{I_{LP}}{I_{in}} = K_B \frac{K_A \cdot \alpha_1 \cdot \alpha_2}{S^2 + K_C \cdot K_A \cdot \alpha_2 \cdot S + K_A \cdot K_B \cdot \alpha_1 \cdot \alpha_2} \tag{10}$$

$$\frac{I_{BP}}{I_{in}} = K_C \frac{K_A \cdot \alpha_1 \cdot S}{S^2 + K_C \cdot K_A \cdot \alpha_2 \cdot S + K_A \cdot K_B \cdot \alpha_1 \cdot \alpha_2} \tag{11}$$

$$\frac{I_{HP}}{I_{in}} = \frac{S^2}{S^2 + K_C \cdot K_A \cdot \alpha_2 \cdot S + K_A \cdot K_B \cdot \alpha_1 \cdot \alpha_2} \tag{12}$$

Where: $\alpha_{1(2)} = \frac{g_{m1(2)}}{C_{1(2)}}$ and K_i is a current gain factor which i=A,B, and C. The center frequency (ω_0) and quality factor (Q) of the second order section, are defined as:

$$\omega_0 = \sqrt{K_A \cdot K_B \cdot \alpha_1 \cdot \alpha_2} \quad \text{and} \quad Q = \frac{1}{K_C} \sqrt{\frac{K_A \cdot \alpha_1}{K_B \cdot \alpha_2}} \tag{13}$$

Then, if $\alpha_{1(2)}$ are equal α (normalized center frequency) and K_{A(B)}=K, the tunable frequency ω_0 will controlled by K or α , and the quality factor Q will defined using $1/K_C$, independently of ω_0 .

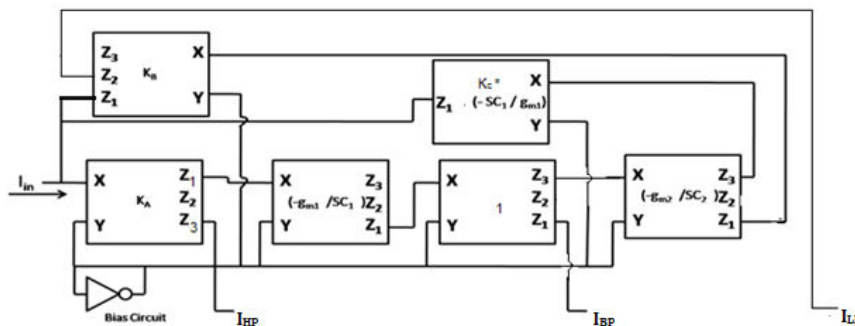
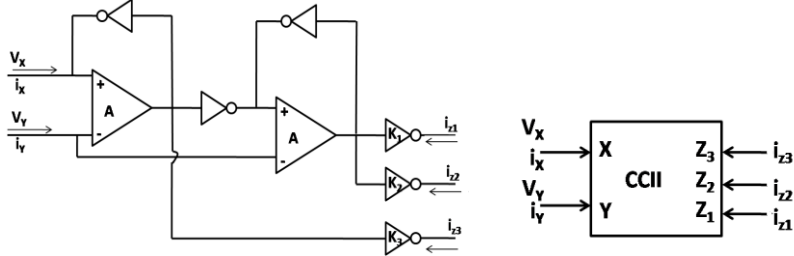


Fig. 10.Current mode second order universal filter.

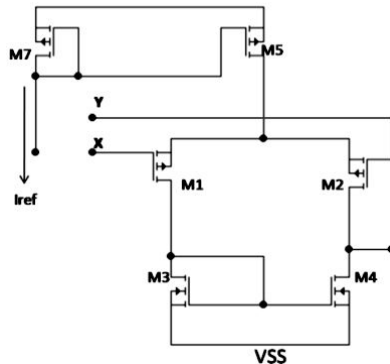
As shown in Fig. 10, each CCII block (K_{A,B,C}) has three outputs. The current gain blocks (K_A, K_B and K_C), are implemented using the current conveyor cell [14] to generate inverting and non-inverting current signals as shown in Fig. 11. The current gain value is the number of CMOS-inverters connected in parallel. Then, I_{in} (I_x), will be mirrored to I_{Z1}, I_{Z2} and I_{Z3} with gain K₁, K₂, and K₃, respectively. For systematic mismatching effect overcome, we emphasis of the all terminal potential are AC ground. Actually, the current gain is number output inverter with respect to the feedback inverter number. Therefore, the programmability of the proposed filter can be achieved using the current gain K_i with different values less or more than one with different sign. The CCII (K_A for example) is characterized as:

$$\begin{bmatrix} I_{z1} \\ I_{z2} \\ I_{z3} \\ V_x \\ V_z \\ I_y \end{bmatrix} = \begin{bmatrix} 0 & -K_1 \\ 0 & -K_2 \\ 0 & +K_3 \\ 10 \\ 10 \\ 00 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \end{bmatrix} \tag{14}$$

The second order filter shown in Fig. 10, is realized for different cut off frequencies and quality factors. The setting coefficients (K_{ij} , $i=A,B,C$ and $j=1,2,3$) and corresponding frequency parameters are in table III, which show the programmability of the corner frequency, note that, K_{C2} is constant (Q is constant). In this CCII block, single stage op-amp is used to save power, as shown in Fig. 11(b).



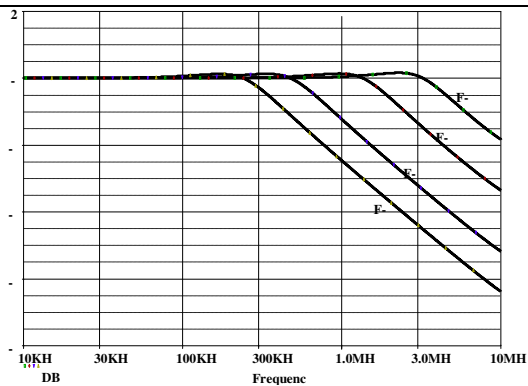
(a). The circuit schematic and symbol.



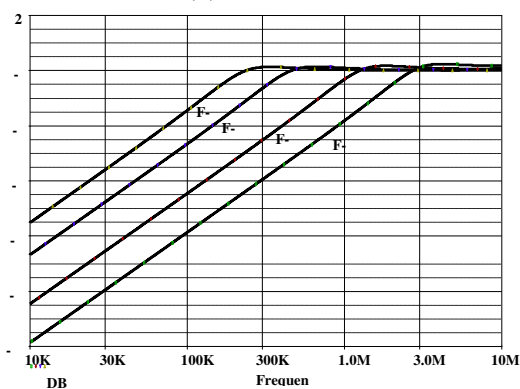
(b). Op-amp schematic.

Fig. 11.The CCII current conveyor [14].

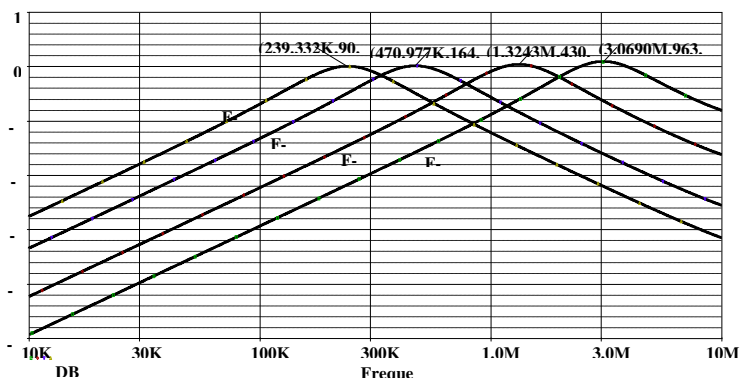
The normalized center frequency ($g_m/2\pi C$) is $\alpha/2\pi$ (11.7MHz). The simulation results (LP, BP, and HP) are shown in Fig. 12. Moreover, the programmability of quality factor, with independently of corner frequency, is investigated as shown in table IV. The simulation results are shown in Fig. 13.



(a). LP filter.



(b). HP filter.



(c). BP filter.

Fig.12.The frequency response of universal filter "cut off frequency programming".

7. Conclusions

In this paper, new topology of current-mode integrator and differentiator circuits have been presented. The proposed circuits are very suitable for LVLP applications. In this topology, the circuits have been used only two analog cells (amplifier, and CMOS

inverter). Therefore, the current mode integrator/differentiator can be implemented all active devices using the FPAA approach. The proposed circuits have been designed and simulated using IBM 0.13 μ CMOS technology transistor parameters. Biquad filter block "current mode universal filter" has been realized and implemented using the proposed blocks. The programmability of the filter has been tested. The designed circuit (filter) is dissipated 10mW power consumption from 1.5V supply. The simulation results illustrated good agreement to theoretical. The results show that the proposed circuits provide high performance with 4% error maximum in corner frequency.

8. Acknowledgment

The author would like to thank the MOSIS Company and IBM foundry for providing him with the model's parameters used in this work.

Table 3.

Simulation parameters.

F-I	K ₁	K ₂	K ₃	F-II	K ₁	K ₂	K ₃
A	1/49	NC	-1	A	1/25	NC	-1
B	1/49	1/49	NC	B	1/25	1/25	NC
C	NC	1	NC	C	NC	1	NC
F-III				F-IV			
A	1/9	NC	-1	A	1/4	NC	-1
B	1/9	1/9	NC	B	1/4	1/4	NC
C	NC	1	NC	C	NC	1	NC

NC " Not Connection.

- SIMULATION RESULTS (Q=1.0).

$f_o = \omega_o / 2\pi$	Simulated "f _{os} "	Calculated "f _{oc} "	$\Delta\{(f_{os}-f_{oc})/f_{oc}\}$
F-I	239KHZ	238.8KHz	0.23%
F-II	470KHz	468KHz	0.7%
F-III	1.32MHz	1.3 MHz	1.847%
F-IV	3.07MHz	2.925MHz	4%

Table4.

Simulation parameters for different Q-factors

F-I	K ₁	K ₂	K ₃	Q _I	F-II	K ₁	K ₂	K ₃	Q _{II}
A	1/25	NC	-1	1/3	A	1/25	NC	-1	1
B	1/25	1/25	NC		B	1/25	1/25	NC	
C	NC	3	NC		C	NC	1	NC	
F-III				Q _{III}	F-IV				Q _{IV}
A	1/25	NC	-1	3	A	1/25	NC	-1	5
B	1/25	1/25	NC		B	1/25	1/25	NC	
C	NC	1/3	NC		C	NC	1/5	NC	

NC " Not Connection".

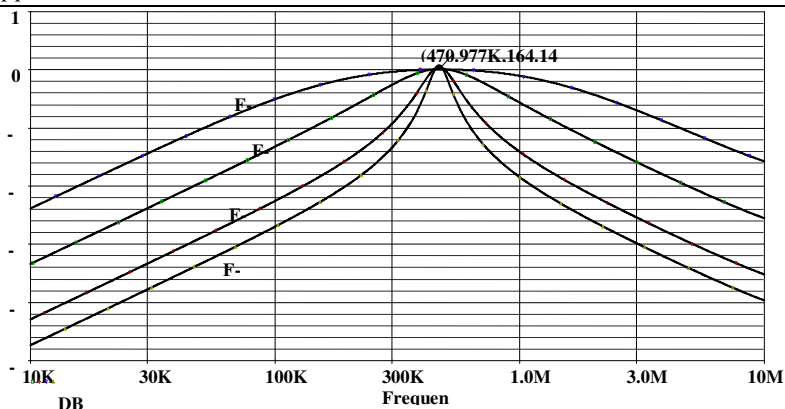


Fig. 13. The frequency response of universal filter at different Q-factor.

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دائرة مكامل ودائرة مفاضل للتيار لتطبيقات الجهد المنخفض والقدرة المنخفضة بأسلوب التيار وتكنولوجيا الـ CMOS

الملخص العربي

البحث يقدم طريقة جديدة لتحقيق مكامل ومفاضل للتيار. الدوائر المقترحة تستخدم دائرة محول التيار CCII المعتمدة علي العاكس نوع CMOS كمصدر للتيار. هذه الطريقة تحقق امكانية عمل تحت جهد مصدر منخفض وتستهلك قدرة منخفضة ايضا وذلك نتيجة للتكوين الداخلي للدوائر المستخدمة. وعلاوة علي ذلك البرمجة للدوائر المقترحة تمت باستخدام دائرة العاكس الرقمي نوع CMOS لذلك تم دراسة العاكس واستنتاج معادلات تصميمه كدائرة تناظرية وليس كدائرة رقمية. تطبيقا لدوائر المقترحة - تم تصميم دائرة مرشح ثنائي الدرجة وتحقيقه. البرمجة للمرشح الثنائي تمت بحيث يكون ان خصائص المرشح (التردد المركزي ω_0) وجودة المرشح ((Q)) غير معتمدة علي بعضها. الدوائر المقترحة والمرشح تم تصميمها ومحاكاتها باستخدام تكنولوجيا CMOS 0,13 ميكرو من IBM.