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FEEDFORWARD COMPENSATION TECHNIQUE FOR COMPARATOR DELAY DISPERSION FOR LEVEL-CROSSING ADCS

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The accuracy of measuring the crossing moment of a given signal to a specific reference voltage plays a crucial role in determining the bandwidth of the signal that could be converted by a level-crossing ADC. This timing accuracy is mainly determined by delay dispersion of the comparator and the accuracy of the time-to-digital converter (TDC) comprising the level-crossing ADC. With the pico-second resolution TDC, the delay dispersion of the comparator became the bottle nick of the design of a high speed level-crossing ADC. This paper presents a comparator with low delay dispersion for level-crossing analog-to-digital conversion applications. The comparator comprises a technique to compensate the delay dispersion caused by variable input overdrive. The whole circuit is composed of three main blocks, namely, conventional comparator, fixed delay block and variable delay block. The variable delay block is controlled such that it implements the inverse overdrive-delay characteristics of the conventional comparator. Therefore, the overall delay dispersion of the circuit is effectively reduced. Using the proposed technique in a level-crossing ADC would enable the sampling of a signal with 6.15X higher frequency than the case of using a conventional comparator keeping the same SNR.

1. INTRODUCTION

Analog to digital converter is an important building block which enables the interfacing between the actual (analog) world and the digital processing environment. The demands for low-power and small area ADC have been the driving forces of developing of the level-crossing ADC (LC-ADC) [1]-[6].

Figure 1 shows the conceptual block diagram of the LC-ADC [7]. It is mainly composed of a level-crossing detector, which is usually a comparator array and an accurate crossing-timing measurement unit, which is a time-to digital converter (TDC). In level-crossing ADC, the signal is sampled when it crosses a threshold level and the time between two consecutive crossings is measured. This is in contrast to conventional ADCs where the signal is sampled with constant time intervals and the acquired amplitude values are approximated with digital numbers. The level crossing approach results in some interesting properties such as absence of quantization noise and possibility of arbitrary placement of quantization levels to accommodate for signal specific properties. In addition, it occupies smaller area and consumes lower power

consumption compared with the conventional ADC. There are many applications for the level-crossing ADC, for examples, in signal processing field; it can be used for interfacing temperature, pressure, vibration sensors and also it can increase the lifetime of cell phones between successive battery charges. Another important field of applications is the biomedical engineering.

The level-crossing ADC has two main blocks: the comparator array and the high precision timing measurement block. Performance of these blocks highly influences the overall performance of the ADC. MATLAB simulations show that when using only 16 quantization levels (4 bits) it is possible to achieve a signal to noise and distortion ratio (SNDR) which is equivalent to 9–10 effective bits of a conventional ADC [6]. However, this sets high requirements on comparator and timer performances.

There are several TDC designs with pico-second resolutions, for example [8]. Therefore the comparator block becomes the bottle nick for LC-ADC. For such application, the key comparator specification is *propagation delay dispersion*. The delay is defined as the time required for the output to reach the 50% point of a transition after the input signal (V_{CMP}) crosses the reference voltage (V_{REF}). This definition assumes that the offset voltage is zero.

In a conventional comparator, the propagation delay varies depending on many factors such as the input overdrive - the difference between the input reference and the compared signals- (ΔV_{OD}), the common-mode level and the slope of the input signal. This variation in propagation delay is called *delay dispersion.*

Figure 2 illustrates the effect of variable overdrive on the timing of the comparator output. That is, for the same crossing moment of the signal under test, the comparator output timing depends on the overdrive voltage. Consequently, large delay dispersion causes a non-recoverable timing error in the reported data. In other words, it deteriorates the signal to noise (SNR) of the output of the level-crossing ADC (LC-ADC). Therefore a low delay dispersion comparator is necessary for LC-ADC.

In [9], the comparator circuit had been developed to decrease the delay dispersion. However, the delay dispersion of the resulted comparator is still large so that the input frequency range is up to 10 MHz. In addition, the relatively large area and high-power consumption of the comparator make it not so attractive for on-chip high-speed signal measurement applications. In [10], a conventional comparator had been used but the input bandwidth is limited to 300KHz.

In this paper, we propose a technique to compensate the delay dispersion of the conventional comparator caused by the overdrive variations. The technique utilizes the characteristics of the first stage differential amplifier to feed forward control the delay of a cascaded variable delay block. Using this technique, the overall delay dispersion is reduced. These results make the proposed technique attractive for the applications such as level crossing analog-to-digital converters and sampling head of the ATE.

The rest of the paper is organized as follows. Section II introduces root causes of delay variation in the conventional comparator. The proposed technique in presented in Section III. The impact of using the proposed technique on the performance of LC-ADC is discussed on IV followed by the conclusion.

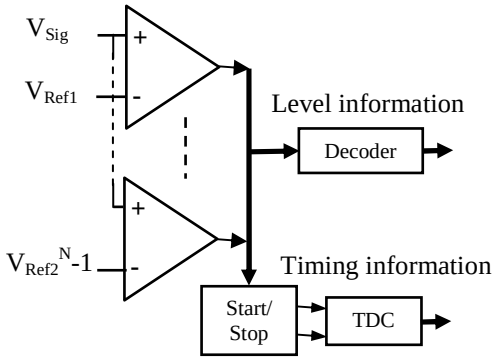

Figure 1: Conceptual block diagram of level-crossing ADC

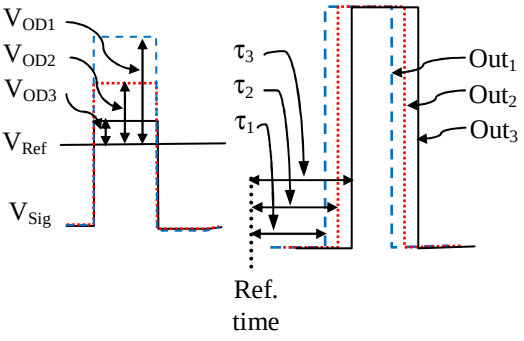

Figure 2: Illustration of effect of overdrive voltage (V_{OD}) on output timing.

2. DELAY DISPERSION IN THE CONVENTIONAL COMPARATOR.

The propagation delay in conventional comparator varies depending on many factors such as the input overdrive (the difference between the input reference and the compared signals), the common-mode level and the slope of the input signal.

Assuming that the comparator is used in a stable temperature conditions, the propagation delay (τ_{pd}) can be given by Equation (1).

$$\tau_{pd} = f(\Delta V_{OD}, V_{CM}, S) \quad (1)$$

Where ΔV_{OD} is the input overdrive voltage, V_{CM} is the common mode level and S is the slope of the input signal. The schematic diagram of the conventional comparator is shown in Figure 3. The comparator is implemented in 65nm technology. For our target application, the inputs voltage difference (ΔV_{OD}) and the common mode level are the most important playing parameters. Hence, the effect of input signal slope is not included in this paper.

The transistor netlist of the conventional comparator shown in Figure 3 is used to study the effect of input overdrive (ΔV_{OD}) and the common mode level (V_{CM}) on the

delay variation by using Hspice simulation. The results are plotted as shown in Figure 4. The figure clearly indicates that the arrival time of the comparator output varies with both the input overdrive and the common mode level. However, the delay strongly depends on the input overdrive more than the common mode level. This variation in propagation delay is called *delay dispersion.* These characteristics make the conventional comparator inappropriate for level-crossing ADC working at high frequency. Specifically, it will cause a non-recoverable timing error in the reported data. Or in the best case, it limits the highest frequency of the signal that can be processed by such ADC. Consequently, a technique is needed to decrease the delay dispersion of the comparator.

3. THE PROPOSED TECHNIQUE

The block diagram of the proposed technique is shown in Figure 5. It is composed of a conventional comparator (represented by difference amplifier stage) followed by a constant and a controllable delay blocks. The whole system represents a comparator with feed forward delay dispersion compensation technique.

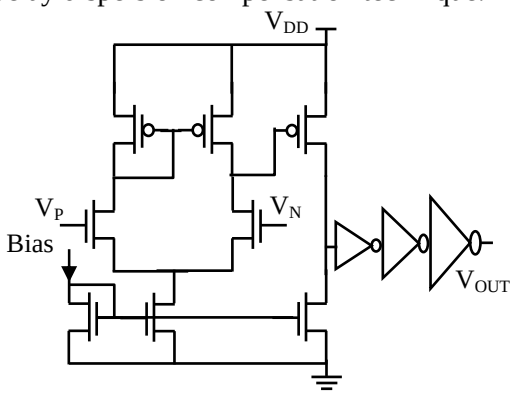

Figure 3: Schematic diagram of the Conventional Comparator

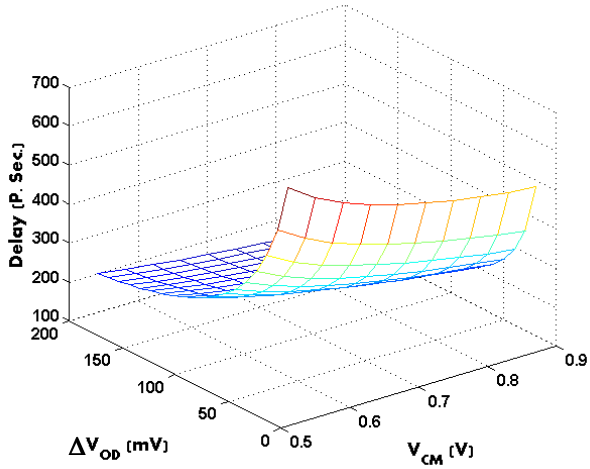

Figure 4: Simulation results of delay variation of conventional comparator versus overdrive voltage (ΔV_{OD}) and common mode level

The operation of the proposed technique can be explained as follows: the overdrive-output transfer characteristics of the differential amplifier can be divided into two main regions, namely the linear region and saturation region. In linear region the output varies linearly with the input overdrive according to the amplifier gain. If the input overdrive is large enough, the amplifier works in the saturation region wherein the output is limited by the supply rails. If the input overdrive is equal to or higher than the value needed to set the differential amplifier in the saturation region, the delay is almost constant as it can be understood from Figure 4. On the other hand if the input overdrive is small such that the amplifier works in the linear region, the delay varies with the input overdrive. Utilizing this criterion, a controllable delay block is used to compensate the overdrive dependent delay variation. The delay of the controllable (variable) delay block is controlled by the output of the differential amplifier stage. When the input overdrive is small, the delay caused by the conventional comparator is large. At the same time, the delay added by the controllable delay is small. Therefore, the total delay of the system is almost constant. In other words, the aim of using the controllable delay block is to implement the inverse characteristics of overdrive-delay variation of the conventional comparator such that the overall delay is kept constant with varying the input overdrive. The constant delay block is inserted to achieve two purposes. The first is to give sufficient time to the variable delay block to adapt its delay according to the input stage. The second is to provide a clean digital signal to the variable delay block.

The technique has been implemented in 65nm technology. The schematic diagram of the technique is shown in Figure 6. The netlist of the design is simulated using Hspice. The simulation results of the propagation delay variation versus the input overdrive are shown in Figure 7. In this figure, there are three curves. From bottom up, the curve shows the Delay-ΔV_{OD} characteristics of the conventional comparator without the compensation technique. The total delay dispersion is about 400 pSec. 310pSec out of this dispersion is in the range of 20mV to 100mV of ΔV_{OD}. The middle curve expresses the delay-overdrive transfer characterizes of the controllable delay block. It shows that the added block tries to implement the inverse delay characteristics of the conventional comparator. Therefore, the overall delay dispersion of the whole circuit is successfully reduced. The delay dispersion of the proposed technique is about 100 pSec in the range of 20mV to 200mV. This means that proposed technique reduced the delay dispersion to ¼ of its counterpart in the conventional comparator working in the mentioned input overdrive range.

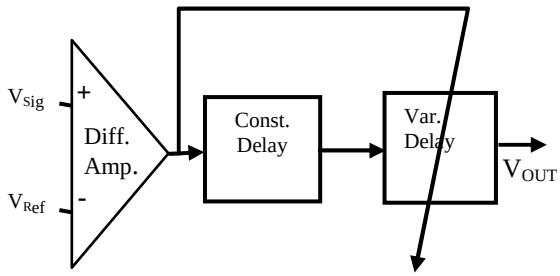

Figure 5: Block diagram of the proposed technique

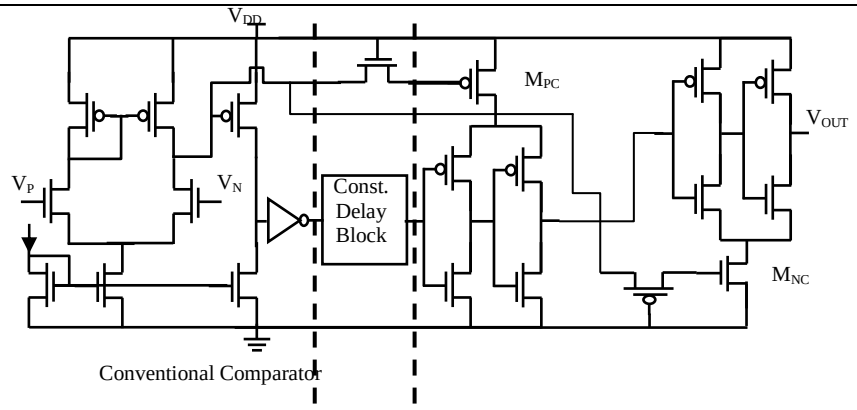

Figure 6: Schematic diagram of the proposed Technique for rising and falling crossing.

The effect of the common mode level (within the designated range) on the delay variation of both conventional and the proposed technique is studied. The results are shown in Figure 8. The results reveal that the proposed technique decreases the overdrive-caused delay variation regardless the common mode level.

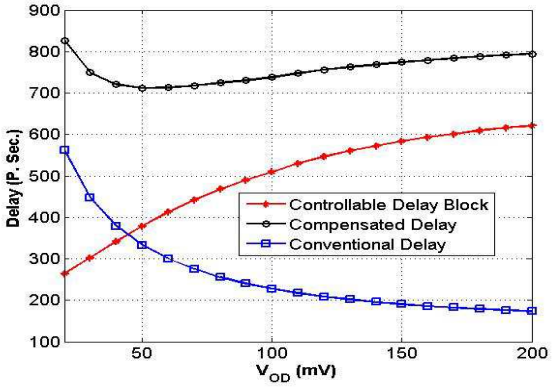

Figure 7: Simulation results of delay variation of conventional comparator and proposed technique versus overdrive voltage (ΔV_{OD})

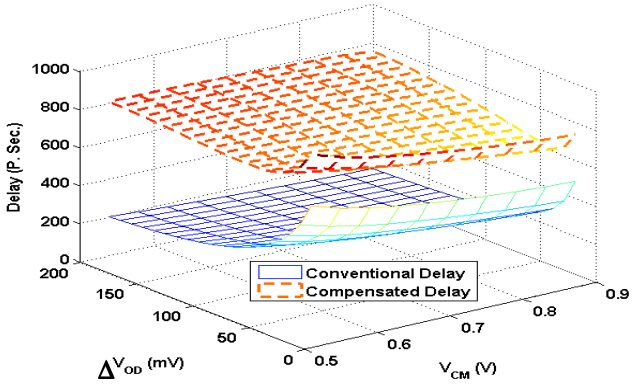

Figure 8: Simulation results of delay variation of conventional comparator and proposed technique versus overdrive voltage (ΔV_{OD}) and common mode level (V_{CM})

4. IMPACT OF THE PROPOSED TECHNIQUE ON LC-ADC PERFORMANCE

In LC-ADC, the SNR depends on timing accuracy of the system and the frequency of the input signal according to Equation (2) [7].

$$SNR = 20logR - 11.2 \text{ dB} \quad (2)$$

Where R is given by $R = 1/(f_{sig}\Delta T)$, f_{sig} is the frequency of the input signal and ΔT is the timing resolution of the system. ΔT is determined by two factors, the first is the resolution of the TDC-the minimum time that can be measured by the TDC . Second is the delay dispersion of the comparator.

Assuming that the TDC has small timing resolution (pico-second order) [11] compared with the delay dispersion of the conventional comparator, the bottle nick will be the timing uncertainty of the comparator; which can be considered as its delay dispersion.

According to the simulation results, using the conventional comparator, the timing resolution (ΔT_{Conv}) is about 400 pSec. On the other hand, using our design the timing resolution (ΔT_{prop}) is enhanced to 100 pSec. Applying these values to the Equation (2), using our design would theoretically increases the SNR with 12.1 dB higher than the case when using the conventional comparator for signals of the same frequency. Alternatively, keeping the same SNR, using the proposed comparator, the frequency of the signal under test could be increased to 4X higher than the frequency of the case when using the conventional comparator.

5. CONCLUSION

A technique for compensating the overdrive-caused delay dispersion of the conventional comparator is presented. The technique is useful for applications such as high-speed level-crossing ADC and sampling head of automatic test equipments (ATEs). The technique is implemented in 65nm technology. The simulation results show that the overall delay dispersion is effectively reduced to ¼ of its counterpart in the conventional comparator. Using the proposed technique in LC-ADC would theoretically increases the SNR with 12.1dB over the case when using the conventional comparator or alternatively increases the bandwidth of the input signal four times larger than the case of using the conventional comparator keeping the same SNR of the output.

6. REFERENCES

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تقنية تغذية أمامية لمعادلة تبعثر زمن التأخير للمقارن فى المحولات الرقمية عابرة المستويات

إن دقة قياس لحظة عبور الإشارة لمستوى جهد معطى تلعب دورا حاسما في تحديد عرض النطاق الترددي للإشارة التي يمكن تحويلها بإستخدام المحولات الرقمية عابرة المستويات (LC-Level-Crossing-ADCs) ((ADC. وهذه الدقة الزمنية تُحدد اساساً بتبعثر زمن التأخير للمقارن و دقة محول الزمن الرقمى (TDC) المكونان لدائرة (LC-ADC). و مع وجود TDC ذو دقة فى حدود الواحد بيكوثانية يصبح تبعثر زمن التأخير للمقارن بمثابة عنق الزجاجة فى تصميم (LC-ADC). و هذه الورقة البحثية تقدم تقنية لدائرة مقارن قليل تبعثر زمن التأخير مقارنةً بالقارن التقليدى و الذى يمكن استخدامه فى تصميم (LC-ADC). ويتكون التصميم المقترح من دائرة مقارن تقليدى و دائرة زمن تأخير ثابت و دائرة زمن تأخير محكومة و التى تستخدم لمعادلة تبعثر زمن التأخير الناتج عن المقارن التقليدى وبهذا يمكن بفاعلية تقليل تبعثر زمن التأخير للدائرة إجمالاً. إن إستخدام التقنية المقترحة فى تصميم (LC-ADC) يمكّن من زيادة تردد الإشارة المراد تحويلها إلى 6.15 ضعف من نظيرتها فى حالة إستخدام المقارن التقليدى مع ثبوت معدل الشوشرة بالنسبة للاشارة (SNR) .