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All-Optical Pseudorandom Binary Sequence (PRBS) Generator Using The Hardlimiters

Tamer. A. Moniem
Communication and electronics dept. MSA University, Egypt

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Abstract

An all-optical pseudo random binary sequence (PRBS) generator is designed using hard- limiters and serially interconnected D flip-flops based on two coupled polarization switches (PSWs). The performance of the circuit is evaluated through numerical simulation to confirm its feasibility in terms of the choice of the critical parameters. The proposed scheme is theoretically demonstrated for a 3-bit and 5-bit degree PRBS and can be extended to higher order.

Keywords: pseudo random binary sequence (PRBS), hardlimiters, D flip-flop, optical gates, SOA.

1. Introduction

Owing to their deterministic nature, ease of construction, reproducibility and attractive statistical properties [1], pseudorandom binary sequences (PRBS) are useful in various fields of digital communications. For instance testing of transmission systems, coding/encoding, cryptography, white noise approximation, bit error rate measurements and code division multiple access (CDMA) are examples of its application [1]. Pseudorandom binary sequence (PRBS) generator is a very commonly used circuit in digital electronics. It has a lot of uses in different applications mainly with digital communications and test pattern generations, such as VLSI testing to generate random test pattern, in image processing block-set to generate random watermark, cognitive radio, cryptography and Steganography, for different noise approximation, bit error rate measurements etc. Its importance is gradually increasing in the field of Opto-electronics due to its simplicity and easy to construct. These applications are not limited to the realization of electronics but can be extended to optics as well, where the scientific community has realized the significant multilateral role of PRBS and has made efforts to produce and process it only by means of light. The main functional unit of a PRBS circuit is called linear feedback shift register (LFSR) which is a group of flip-flop connected in series with some feedback mechanism. Depending on the number of flip-flop used in the circuit it can produce same number of output bits in an instance. The total number of instances it can generate is called maximal length sequence (L) which can be easily obtained using finite field or Galois field theory with proper tapping. There is exactly one finite field up to isomorphism of size p^k for each prime p and positive integer k. The multiplicative group of the field is a cyclic group. The signal takes out from a point to provide feedback connection is called tapping.

In case of considering all optical linear feedback shift register (LFSR), the design is not exactly the same with its electronics counterpart. Perhaps it has higher degree of

complexity due to the use of optical source as a signal carrier. Here we need to control the flow of signal in terms of light, to make synchronization of different signal. These signals are necessary to insert different delay elements in terms of optical fibres in a proper recirculation loop configureuration. Whereas the simulation process and experimental setup for such an approach are complex to realize from all angle as compared to digital counterpart. Thus to overcome this complexity, proper design should be required. Knapp et al demonstrated 2^7-1 length of 40 Gb/s PRBS circuit based on SiGe bipolar technology [2]. Kim et al also demonstrated 45 Gb/s PRBS using the same component [3]. Nor type LFSR model is also designed by Ahmad [4]. Poustie et al presented 45 Gb/s PRBS using terahertz optical asymmetric demultiplexer (TOAD) based switch [5]. Zoiros et al also showed the design of all-optical PRBS using shift registers [6] and TOAD based D-latch arrays [7]. Fatome et al suggested 42.66 Gb/s PRBS using differential phase shift keying (DPSK) technique [8]. Recently Berrettini et al presented all-optical PRBS circuits using SOA-based loop memories [9].

In order to overcome the electronic bottleneck and fully exploit the advantages of fibers, it is necessary to move towards networks, where the transmitted data will remain exclusively in the optical domain [5]. Electrical to optical and optical to electrical conversion limit the speed of optical networks. So that, an all-optical PRBS is introducing to exploit the speed and increase the performance of the optical network**.**

In this paper we have implemented an all optical PRBS generator exactly in a same fashion like its electronic counterpart with minimum complexity by using D flip-flop. Where Hardlimiter based Demultiplexer has been used as a basic element of a D flip-flop [10-11]. According to the field theory all flip flops are connected in series one after another. All tapped signal has been XOR-ed using Hardlimiter based all optical AND and XOR gate [12].

2. All Optical AND and XOR gate using Hardlimiters

The structure shown in Figureure 1 consists of alternating layers of materials, each one possesses a Kerr non-linearity. The refraction index of such a material can be expressed as [13, 14],

$$n=n_0+n_{nl}I \qquad (1)$$

where, n_0 is the linear index, n_{nl} is the Kerr coefficient and I is the local intensity of light The equation govern the relation between incident intensity (I_{in}) and transmitted intensity

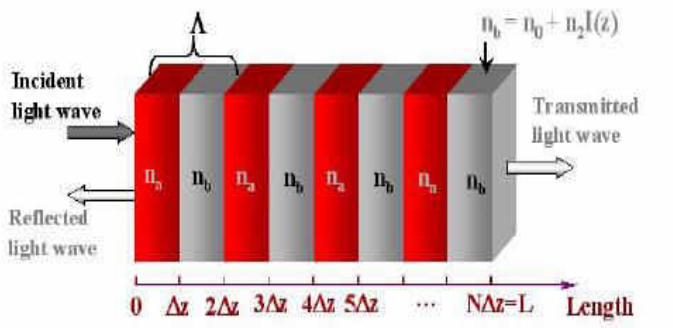


Figure 1 Schematic diagram of a simple nonlinear periodic structure with periodicity Δz

(I_{out}) can be expressed as [12, 13, 14]

$$I_{out} = \begin{cases} 0 & for \quad I_{in} < a < (1 - \frac{1}{2^N}) \\ a[2^N (I_{in} - 1) + 1] & for \quad a(1 - \frac{1}{2^N}) < I_{in} < a \\ a & for \quad I_{in} > a \end{cases} \tag{2}$$

Where **a**= $(n_{01}-n_{02})/(n_{nl1}-n_{nl2})$ (3)

Figureure 2 illustrates the use of the proposed limiter to construct an all optical XOR and AND gates. Inputs A and B gets combined into a single beam. The transmitted intensity is defined as the O1 output and the reflected value as the output O2 [11, 12]. We bias the hardlimiter at a=2. If one of the inputs is 0 and the other 1, the output at O1 is 0 and at O2 is 1. If both A and B inputs have the value of 1, the transmitted output equal to 1 and 0 is reflected. If both A and B inputs have the value of 0, a 0 is transmitted and a 0 is reflected. Thus, O1 yields the result of an AND operation and O2 the result of a digital XOR. The intensity value 2 output of O1 (AND) must be normalized to yield a digital output.

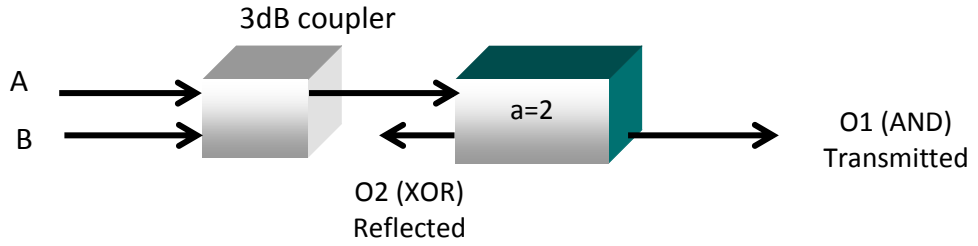


Figure 2 XOR and AND gates, for two inputs A and B with hardlimiter at a=2

3. All Optical De-Multiplexer using Hard limiters

A digital De-multiplexer is a combinational circuit which has one input and 2^n outputs, where n is the number of select line. Depending on the value of select line the input signal get transfer to a particular output line. De-multiplexer is another form of decoder. T. A. Rahman had designed an all optical 2:4 decoder circuit of two inputs and four outputs [12]. Here as shown in figureure 3 we have consider same principle as [12] to design a 1:2 De-multiplexer. The select line A is first amplified by using optical amplifier (EDFA) then divided into two signals, one signal directly fed into the D flip-flop and the other one fed to 3 dB coupler. The input signal (always set at logic 1) get combined with a signal coming into the coupler and form a single beam which fed into limiter (Hardlimiter is biased with a=2). The output of the hardlimitter is fed to delay elements to synchronize all outputs. When the selection line A have 0 logic then D_0 line get selected and logic 1 comes out through this line whereas D_1 line produce 0 logic value. In another case when A have logic 1, the output at D_1 become logic 1 and output at D_0 becomes logic 0. So, we can conclude that this circuit is behaving like an all optical De-multiplexer circuit. This will be used for further operation in our design.

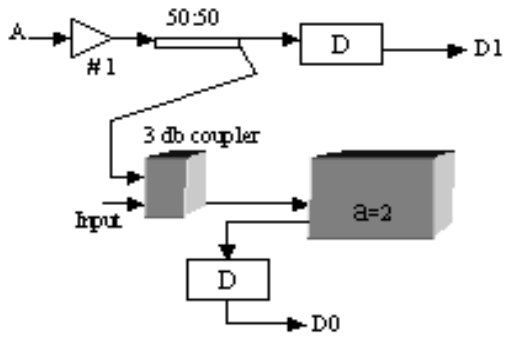


Figure 3 All optical 1:2 De-multiplexer

4. All Optical D Flip-Flop

The structure of the all-optical flip-flop memory is depicted in Figureure 4 as designed in reference [11]. It consists of two coupled polarization switches (PSWs). The first PSW1 output light is injected into the second PSW2. Hence, the light that PSW1 outputs acts as a saturating control signal for SOA2 that can suppress PSW2 and the light that PSW2 outputs can act as a saturating control signal for the SOA1 to suppress PSW1 [11, 15]. Optical pulses are injected into PSW1 via Port I of PBS (polarization beam splitter) to set the flip-flop in State1 [11]. The optical pulses are injected into PSW2 via Port II of PBS to reset the flip-flop in State 2. The ports of set and reset are connected to the output of all-optical DMUX 1*2 with input connected to laser source of 1 mw power and wavelength of 1551 nm. The selection A of DMUX is considered as the input D of the flip-flop. So, if D=1, the laser beam applied to set port to set flip flop and if D=0, the laser beam applied to reset port to reset flip flop.

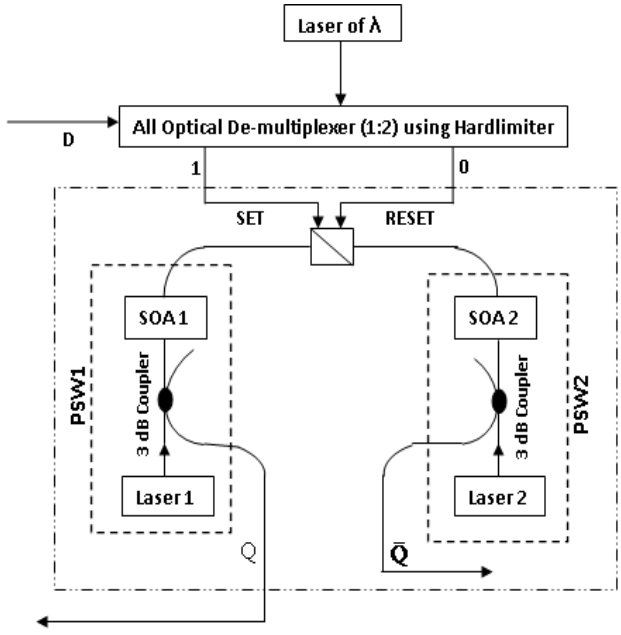


Figure 4 All optical D flip-flop

5. Pseudorandom Binary Sequence (PRBS) Generator

The m bit shift register have less than the maximum of 2^m normal states. An n bit Linear Feedback Shift Register (LFSR) can have 2^m-1 states, almost the maximum. Such a counter is often called maximum length sequence generator. The design of LFSR is based on finite field theory. The operation of an LFSR counter corresponds to operations in a finite field with 2^m elements.

Figureure 5 shows m-degree two taps LFSR circuit. Here last memory unit (m-tap) and the k-th memory unit (k-tap) are fed to XOR gate. The feedback polynomial of this circuit is:

$$f(x) = x^m + x^k + 1 \tag{4}$$

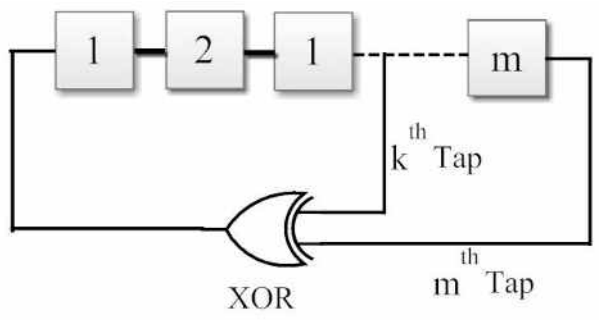


Figure 5 LFSR with feedback polynomial $f(x) = x^m + x^k + 1$

The input bit of the linear feedback shift register (LFSR) is a linear function of its previous state. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its previous state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and a very long cycle. LFSR have following properties: [6]

- The expression of the feedback polynomial as shown in equation (4) depends on the “tapping” position. There are millions of possible tapping’s. The proper "tapping" point is well defined by Galois field theory to generate the maximum length sequence.
- The initial state must be different from all zeros (i.e. 000…).
- The number of feedback taps must be even or shift register will cycle with all 1s state (i.e. 111…).

To implement a PRBS circuit with period 2^3-1 requires 3 memory units and the selection of two taps, the last and the 1st or 2nd. All of these possible tap sections corresponds to the equivalent characteristics trinomial [16]

$$x^3 + x^i + 1, \text{ where } i \in \{1, 2\} \tag{5}$$

Figureure 6 presents the overall construction of all optical pseudorandom generator of length m=3, it is consists of 3 cascaded all optical D flip flops, and a set of optical Hardlimiter AND gates and one XOR gate which equivalent to module 2 adder. SOA's (semiconductor optical amplifier) are used to compensate the losses of the cascaded connections between flip flops and optical couplers 50:50 by adjusting the SOA [17] current injection from 240 mA to 270 mA for different SOA's.

The logical expression of different outputs can be expressed as:

$$\begin{aligned} S_0 &= \left(S_1 \oplus S_3\right) \\ D_1 &= CK \cdot S_0 \\ D_2 &= CK \cdot S_1 \\ D_3 &= CK \cdot S_2 \end{aligned} \tag{6}$$

' $\oplus$ ' and ' $\cdot$ ' indicate the XOR and AND operation respectively.

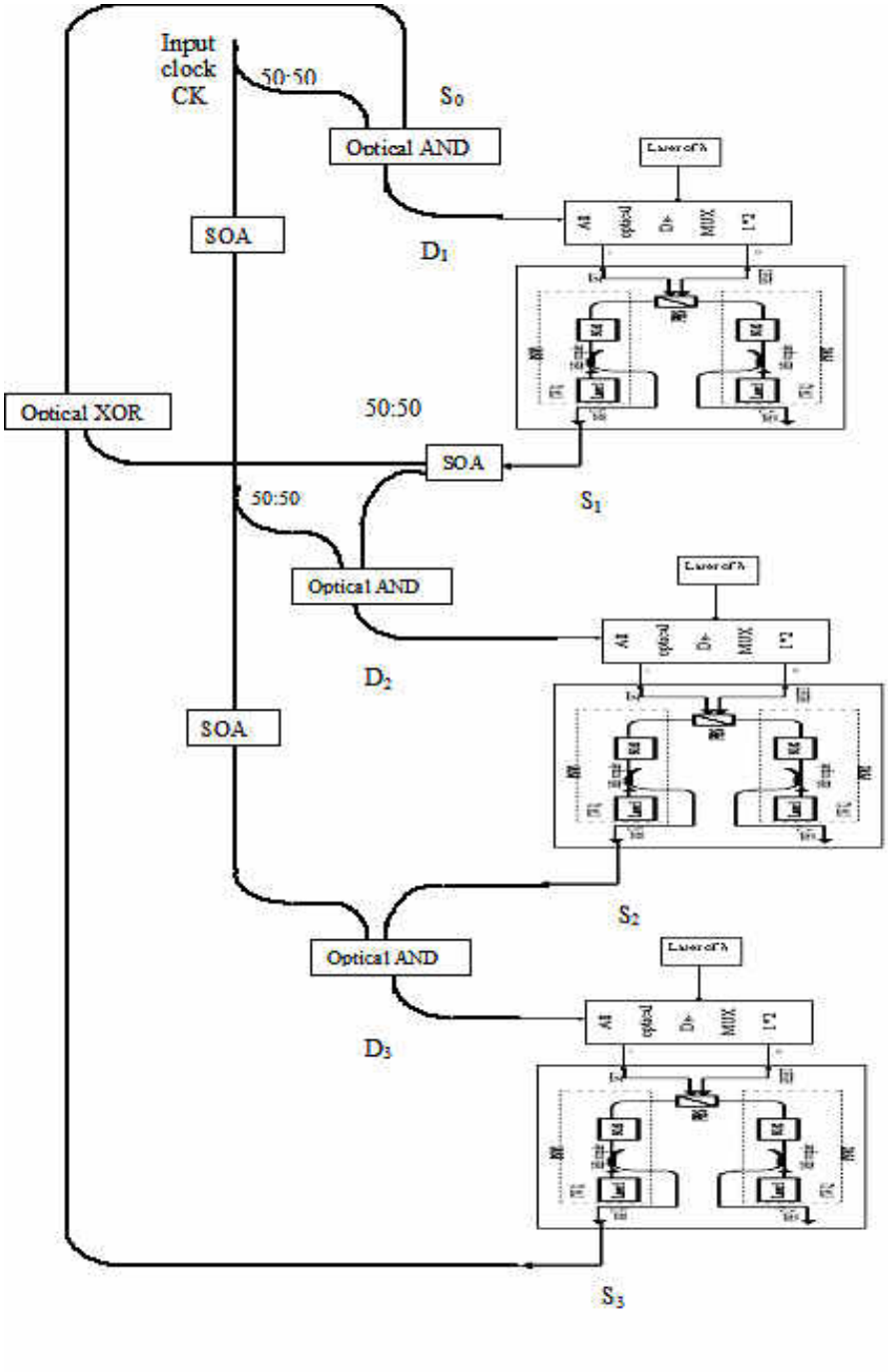


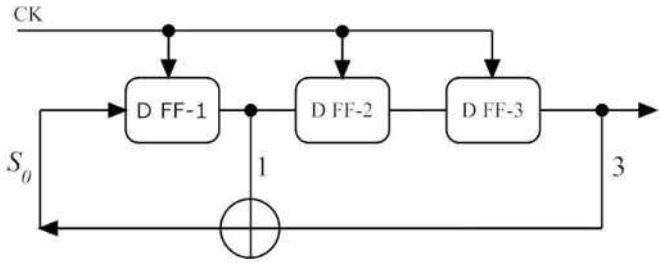
Figure 6 All-optical Linear Feedback shift register of length m=3 with feedback Tap [3, 1]

This type of PRBS has the feedback polynomial $\left(x^3 + x + 1\right)$. The successive state from the proposed circuit is shown in Figureure 7. Let first case is $S_1\ S_2\ S_3$ = 1 0 0. The successive states are presented in the Figureure 7. Here we see that the D FFs have gone through states 100, 110, 111, 011, 101, 010 and reaches 001. Then the repetition happens with period 2^3-1 = *7* and the output sequence is …0011101, 0011101… . Thus an infinite periodic sequence that repeats every 7 bits can be generated. The 7 successive subsequences of length 7 obtained from the infinite sequence as given below.

$$T = \begin{vmatrix} 0011101 \\ 1001110 \\ 0100111 \\ 1010011 \\ 1101001 \\ 1110100 \\ 0111010 \end{vmatrix} \tag{7}$$

If all S_i s (i = 1, 2, 3) are zeros (i.e. $S_1\ S_2\ S_3$ = 0 0 0) the circuit do not operate [7]. This condition should never happen.

Figureure 8 is the extended version of the above concept with m=5. It is consisting of 5 cascaded all optical D flip flops, and a set of optical Hardlimiter AND gates and one XOR gate which equivalent to module 2 adder. We also have simulate the above two circuit and good responses are achieved as shown below.



State number	State			XOR output	Remarks
	S_1	S_2	S_3	$S_0 = (S_1 \oplus S_3)$	
1	1	0	0	1	Initial
2	1	1	0	1	
3	1	1	1	0	
4	0	1	1	1	
5	1	0	1	0	
6	0	1	0	0	
7	0	0	1	1	final
8 = 1	1	0	0	1	Repeat
9 = 2	1	1	0	1	Repeat

Figure 7 Successive states from the 3 bit degree PBRS circuit.

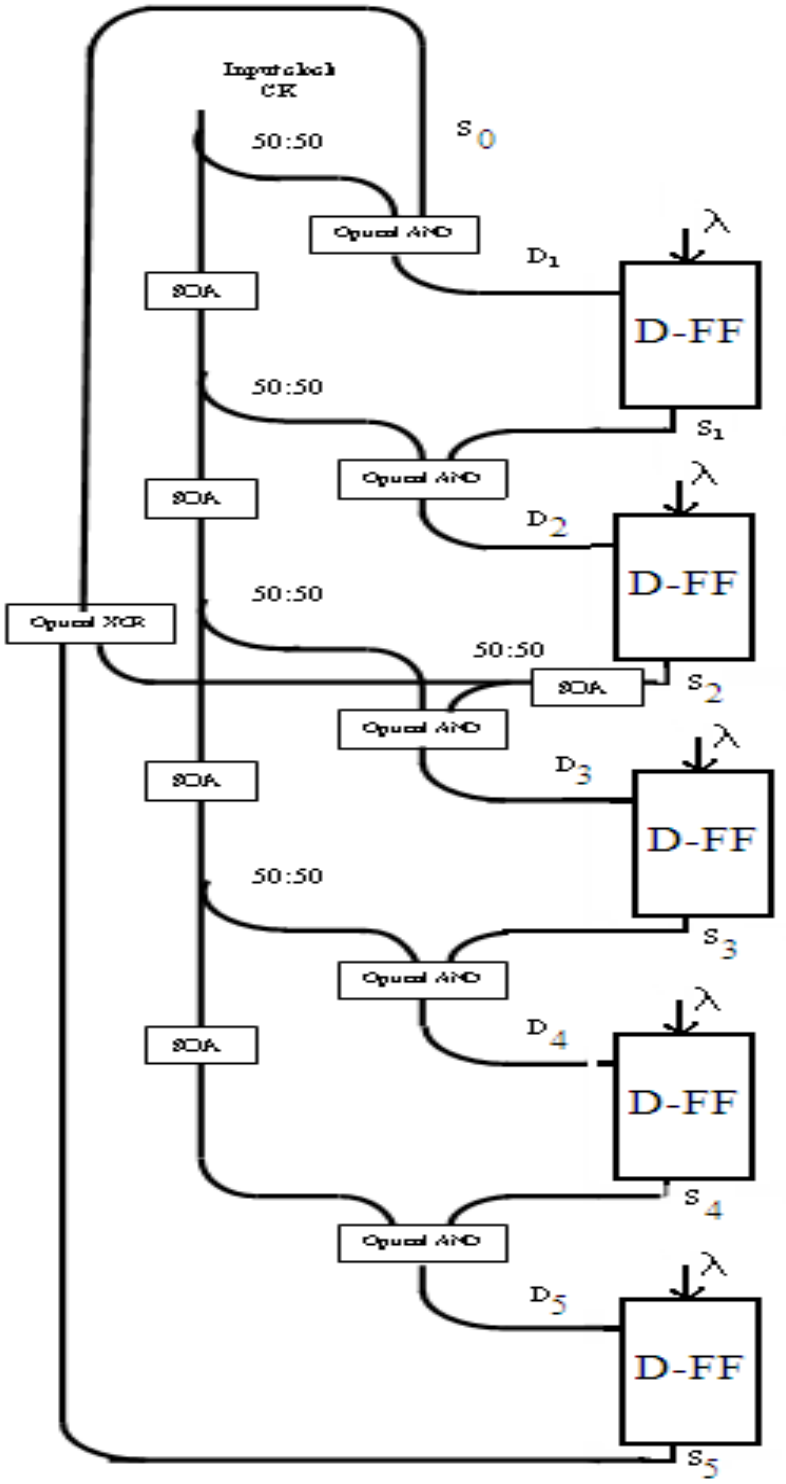


Figure 8 All-optical Linear Feedback shift register of length m=5 with feedback Tap [5, 2

6. Simulation and Results

The PRBS is designed and numerically simulated using Beam Prop method V.7 and opto-wave simulation program V.2 at an operation speed of 100 MHz. The wavelengths of each flip-flop are 1550 nm for λ1 and 1552 nm for λ2. There is an external light input at wavelength of 1559 (λ3) is injected as clock pulse (ck). The optical clock pulses to change the state shift register were injected every 0.1 nanosecond, where the parameters used in the simulation at these wavelengths for SOA are shown in table 1. The overall optical fiber used is a single mode optical fiber with overall length assumed equal to 15 m for PRBS of m=3 and 21 m for PRBS of m=5. This long fiber effects on the time taken and the speed of division operation. So, the photonic integration technologies are used for increasing the overall speed of operation [15, 17], where the optical integrated circuit reduces the length and the size of optical components to sub nanometers which perform a high speed of optical processing operations [18, 19].

The waveform of simulation results for each flip flop output in the two circuits of PRBS for m=3 and m=5 are shown in figureure 9 and figureure 10 respectively with initially binary code 100 and 01000.

Table 1 The parameters of SOA used in simulation

Parameter	Symbol	Value
Injection current of SOA	I	240-270 mA
Unsaturated single- pass amplifier gain	Go	17-23 dB
Line-width enhancement factor of SOA	α	7.25-7.5
Gain recovery time	τe	270 Ps
Saturation energy of the SOA	Esat	1.21-1.23

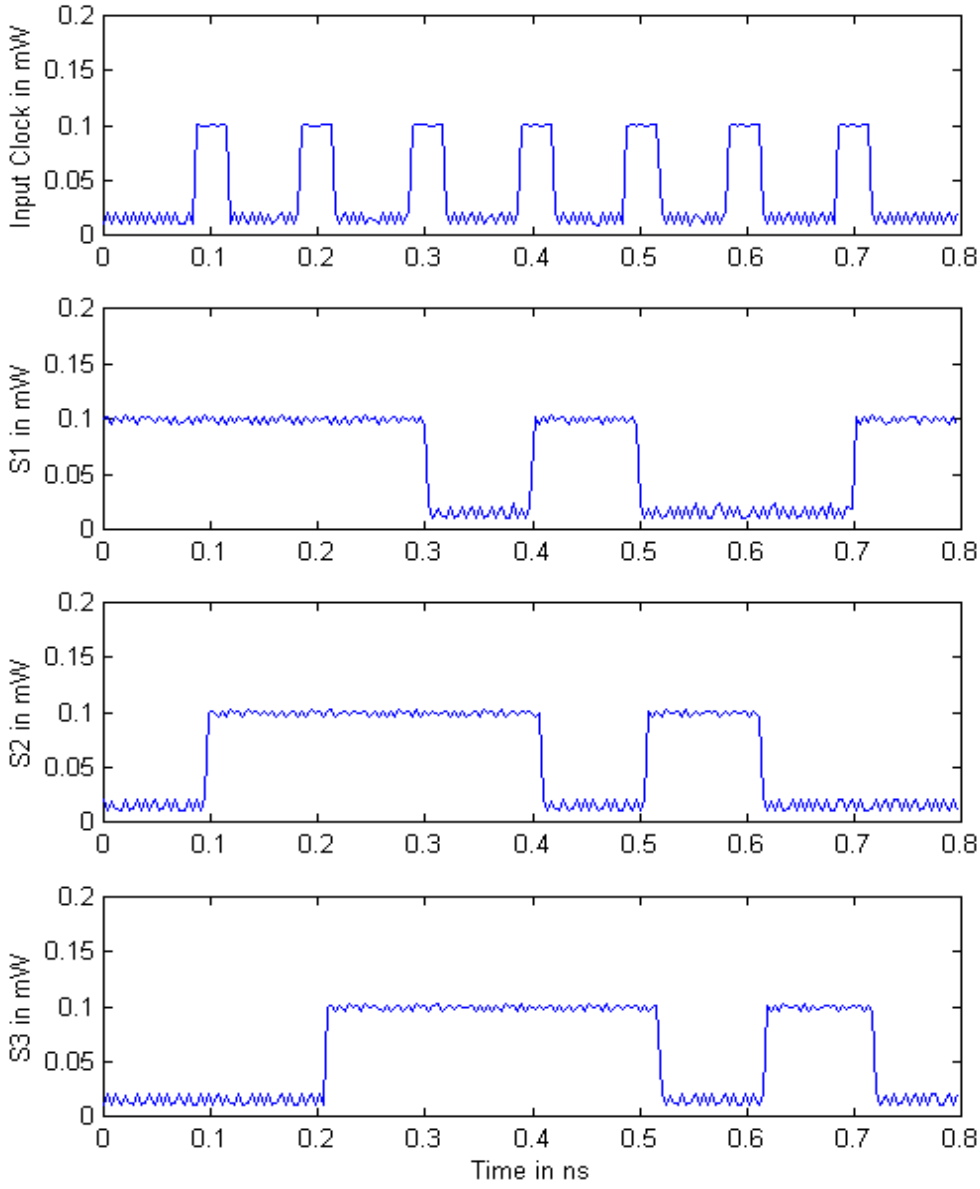


Figure 9 Numerical Simulation of m=3

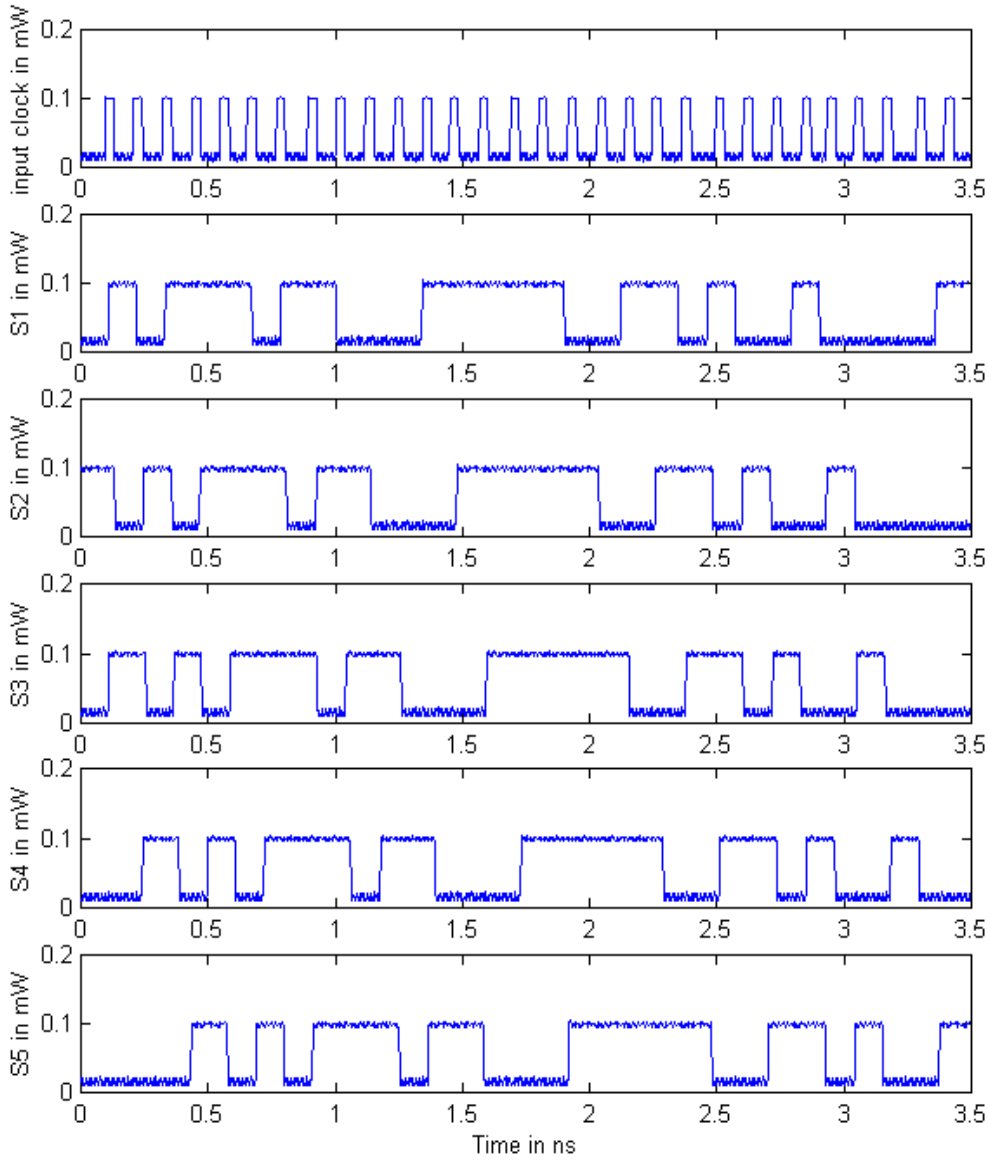


Figure 10 Numerical Simulation of m=5

7. Conclusions

In this paper, we have proposed and described all-optical schemes for pseudo random binary sequence (PRBS) generator of 3 and 5 bits using all optical D flip flops and set of optical gates. This all-optical scheme can easily be extended by means of additional D flip-flops base on two coupled polarization switches. Numerical simulation results confirming the described method are given in this paper. The theoretical model is developed and the numerical results are obtained which are useful in future all-optical computing and information processing. All-

optical system computation eliminates the conversion from optical to electrical and vice versa. Accordingly, the latency is smaller than that using electrical digital computation. The speed of the flip flops is very high and reached experimentally and simultaneously to 100 MHz -600 MHz, but this speed could be increases by using the techniques of building integrated Bragg gratings and optical fibers on SOI ridge waveguides [18, 19].

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تصميم مولد ثنائي متسلسل زائف باستخدام المحدد الصلب

الورقة البحثية تقدم تصميم لمولد ثنائي متسلسل زائف ضوئي باستخدام المحدد الصلب ومجموعه من الدلتا المتارجحه النطاطة التي يعتمد تصميمها على المفاتيح الثنائية الاستقطاب. وتقدم الورقة البحثية في النهاية تقييم لأداء المولد عن طريق نظم المحاكاة الضوئية مع اختيار العوامل المناسبة والمطابقة للواقع. والمخطط المقترح للمولد سيستخدم لتصميم لمولد ثنائي متسلسل زائف ضوئي من درجتي ال 3 بت وال 5 بت مع إمكانية استخدامه لدرجات اعلي.