# HIGH LINEARITY CMOS VARIABLE GAIN AMPLIFIER FOR UWB APPLICATIONS

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## ABSTRACT

A large dynamic-range Variable Gain Amplifier (VGA) suitable for Ultra Wide Band (UWB) applications is presented. The VGA is composed of three programmable variable gain amplifier stages followed by an output buffer. Such wide bandwidth allows our proposed VGA to be used in multi-standard protocols. Power reduction is developed for the variable gain amplifier stages. Thorough analyses of the mid-band gain and noise are presented; and design tradeoffs are carefully handled. The VGA circuit is designed and simulated in 0.13 µm IBM-CMOS process; the overall VGA with buffer consumes 25 mA from a 1.5 V supply. The VGA achieves 54.5 dB dynamic-range (DR), 17.6 dBm IIP3, -42.31 dB THD at peak-to-peak differential output voltage of 1 V, and frequency 400 MHz. Moreover; the proposed circuit reports a good noise performance; the average integrated noise is 121.6 nV/√Hz at minimum gain of -0.5 dB.

*Keywords:* Automatic Gain Control (AGC), Variable Gain Amplifier (VGA), Digitally-controlled Variable Gain Amplifier (DVGA), Buffer, CMOS Analog Integrated Circuits, Low Voltage, Wide Bandwidth.

## 1. Introduction

**T**he variable gain amplifier (VGA) is an indispensable building block to maximize the dynamic range of modern wireless communication systems [1], [2]. It is also widely used in medical equipment, hearing aids, disk drives, and so on [3]–[5]. A VGA is typically employed in a feedback loop to realize automatic gain control (AGC). The VGA of an AGC loop is used to control the transmission signal power or to adjust the received signal amplitude. There are two possible approaches to control the gain of the VGA. One is to build a discrete gain step VGA with a digital control signal [6], [7]; and the other is to design a VGA controlled by an analog gain- control signal [1]–[5]. Basically, digitally-controlled VGAs use binary weighted arrays of resistors or capacitors for gain variations whereas analog-controlled VGAs adopt a variable transconductance or a variable resistance to control the gain. VGA circuits based on various technologies such as bipolar, BiCMOS, and CMOS have been introduced in the literature (e.g. [1]–[4]).

An important VGA requirement is to have a linear-in-decibel gain control characteristic, where the gain of the VGA changes exponentially with the control signal. The exponential gain control is required to achieve a wide dynamic-range and to maintain the AGC loop settling-time independent of the input signal level [8].

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Another important aspect of a wideband VGA is to attain a large bandwidth. There are many systems for high-speed data communications such as ultra-wideband (UWB) systems, wireless local area networks (LANs), and Bluetooth. These systems provide a high data rate with relatively low power consumption in short-range wireless communications. For high-speed data communication, the bandwidth of a VGA must be very wide. Therefore, a wideband VGA is a key component.

While the density of the devices in Nanoscale technology is continually increasing, the interconnect lines across a chip increase significantly. Such long interconnects mandate the requirement of driving large capacitances [12]-[15]. Moreover, in some situations, circuits should have large fan-out. For these reasons, buffers are frequently used in analog and mixed signal circuits. Well-designed buffers should drive large capacitive load with wide bandwidth, minimum power consumption, low distortion, and low loading effect.

In this paper, we propose a new highly-linear wideband variable gain amplifier VGA. Our VGA parameters are compared to [17] – [20] to clarify the merits of the proposed circuit. It could obtain a high linearity, wide bandwidth, and large dynamic-range with large capacitive load and high swing.

Section II describes the architecture of the proposed wideband VGA supported by VGA-cell analysis. The design of the main blocks in the VGA is also explained. Noise and linearity performance of the VGA are analyzed. The implementation and simulation results are presented in Section III. The results are also analyzed and discussed. Conclusions are given in section IV.

## 2. Wideband CMOS variable gain amplifier

The proposed variable gain amplifier VGA, as shown in **Fig. 1**, consists of a number of variable gain amplifier stages (cells) followed by a buffer to drive the load. A binary control-word is used to control the gain of the variable gain amplifiers. The bandwidth of such variable gain amplifier cell should be so wide that the overall bandwidth of the whole VGA design is achieved. In this section, we introduce a three-stage configuration to implement the VGA with wide bandwidth, in which all VGA-cells are identical. The Variable Gain Amplifier (VGA)-cells implementation is considered and analyzed here. A novel VGA-cell, based on the Flipped Voltage Follower (FVF) [11] technique, is proposed with modifications to increase the headroom for the output swing and to enhance the transconductance of the VGA-cell. A new topology for the output buffer is also described and analyzed.

### *2.1. Variable gain amplifier cell*

The complete circuit of the proposed VGA-cell is shown in **Fig. 2.** It demonstrates the signal-processing circuit, the common-mode-feedback circuit, and the bias circuit.

The VGA-cell consists of a CMOS differential amplifier, in which the $R_f$ and $R_s$ are used to vary the gain. Cs is inserted to widen out the bandwidth. $M_1$ and $M_2$ are used to transfer the differential-voltage signal across $R_s$, which in turn is converted into differential-current flowing through $M_3$ and $M_4$. The differential signal current is mirrored to the output branches through $M_5$ and $M_6$. $M_7$ and $M_8$ are connected in Wilson current-mirror like-connectivity to define drain voltage of $M_1$ and $M_2$; and to provide larger headroom for the swing at these points in contrast to [11]. It also provides large output resistance at the output nodes $V_{OP}$ and $V_{OM}$. This VGA-cell is typically used to get the coarse and fine steps by controlling $R_s$ and $R_f$, respectively.

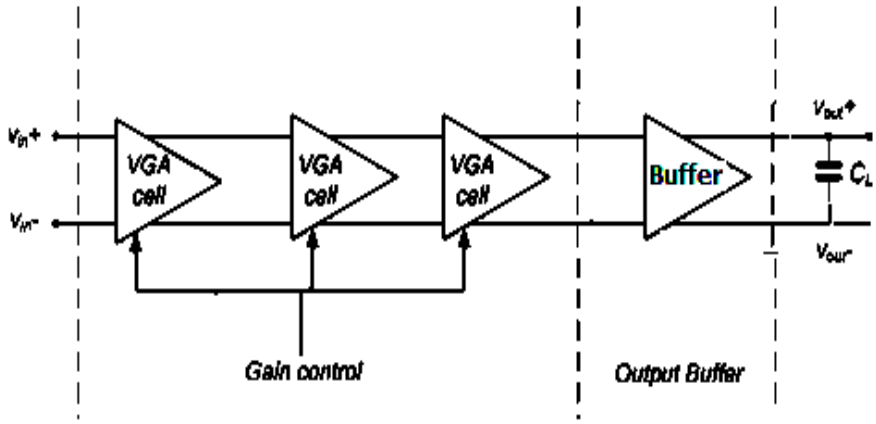


**Fig. 1.** Architecture of the overall VGA.

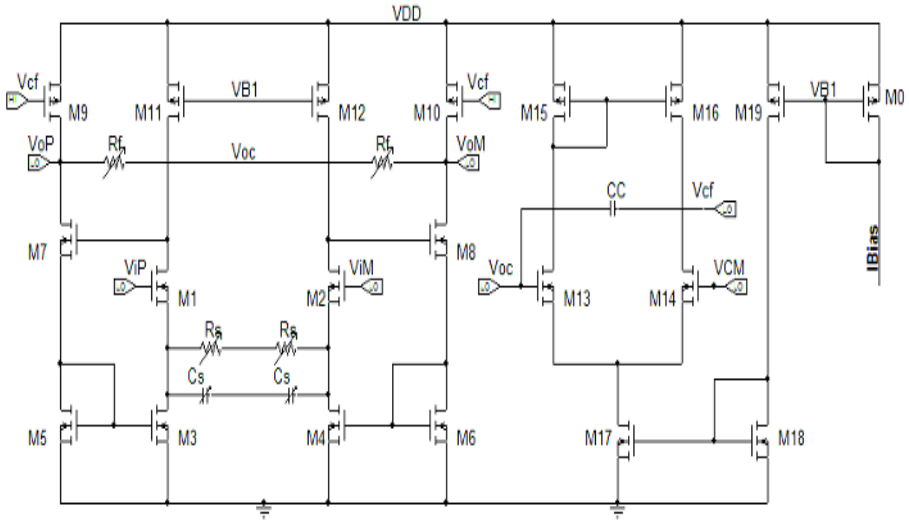


**Fig. 2.** Schematic diagram of the proposed VGA-cell.

The output voltage ($V_{OP}$) half-circuit of the low-frequency small-signal model for the differential amplifier is shown in **Fig. 3**. The output voltage can be written as,

$$V_{oP} = -g_{m5} V_{gs3} (R_f \,//\, r_{o9}) \qquad (1)$$

where $g_{m5}$ is the transconductance of $M_{5\text{-}6}$, $V_{gs3}$ is the voltage between gate and source of $M_{3,4}$, and $r_{o9}$ is the output resistance of the transistor $M_{9\text{-}10}$. $r_{o5}$ is ignored, compared to $1/g_{m5}$. The input voltage $V_{iP}$ of the differential amplifier is then,

$$V_{iP} = V_{gs1} + (I - g_{m3} V_{gs3})(R_s \,//\, r_{o3}) \qquad (2)$$

where I is the current flowing into $r_{o11}$.

$$I = \frac{g_{m1} r_{o1} V_{gs1} + g_{m3} (R_s \,//\, r_{o3}) V_{gs3}}{\left[(R_s \,//\, r_{o3}) + r_{o1} + r_{o11}\right]} \qquad (3)$$

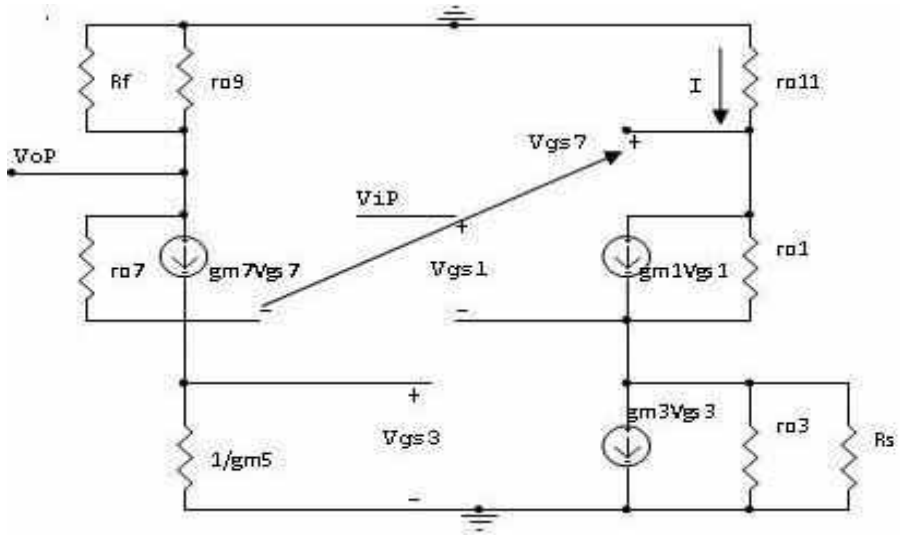


**Fig. 3.** Small-signal model of VGA circuit.

Applying KVL on the output branch, $V_{gs7}$ can be calculated as,

$$V_{gs7} = \frac{\left[1 + g_{m5}(r_{o7} + (R_f \,//\, r_{o9})\right] V_{gs3}}{g_{m7} r_{o7}} \qquad (4)$$

On the other hand, $V_{gs3}$ can be related to $V_{gs7}$ as,

$$V_{gs3} + V_{gs7} = -I r_{o11} \qquad (5)$$

Using equations (1) through (5) and doing some mathematical manipulation, we can calculate the output voltage gain $A_V$:

$$A_V \equiv \frac{V_{oP}}{V_{iP}} = \frac{(R_f \,//\, r_{o9})}{(R_s \,//\, r_{o3})} \left[ \frac{1}{\left( \frac{g_{m3}/g_{m5}}{1+\frac{(R_s \,//\, r_{o3})}{r_{o1}+r_{o11}}} \right) + \left[\frac{X}{A}\right] \left( \frac{1+\frac{g_{m1} r_{o1} (R_s \,//\, r_{o3})}{[(R_s \,//\, r_{o3})+r_{o1}+r_{o11}]}}{g_{m5}(R_s \,//\, r_{o3})} \right)} \right] \tag{6}$$

$r_{o11}$ represents the resistance of the current source. If $r_{o11}$ is relatively large, the output voltage gain $A_V$ can be approximated as,

$$A_V \equiv \frac{V_{oP}}{V_{iP}} = \frac{(R_f \,//\, r_{o9})}{(R_s \,//\, r_{o3})} \frac{g_{m5}}{g_{m3}} \tag{7}$$

It is worthy to mention that the effective transconductance seen by the degeneration resistance $R_s$ is enhanced resulting in small voltage loss from the input to the source of $M_1$. As seen from (7), the voltage gain $A_V$ is independent of transistor parameters except for $r_{o9}$, and $r_{o3}$. In reality, $R_f$ and $R_s$ are chosen much smaller than $r_{o9}$, and $r_{o3}$, respectively. $A_V$ can then be approximately expressed as,

$$A_V \cong \frac{R_f}{R_s} n \tag{8}$$

where n is the ratio ($g_{m5}/g_{m3}$). As a result, the gain of the circuit is stable across process corner variations. In our design, n is chosen to be equal to unity whereas the ratio $R_f$ / $R_s$ should be designed to implement linear-in-dB gain.

## *2.2. Noise analysis of the proposed VGA*

Half of the differential amplifier with equivalent noise sources is shown in **Fig. 4**. The drain-source noise current generators of MOSFETs are considered. For noise sources of $M_{3,4}$ and the resistance $R_s$, the total output noise can be calculated as [20],

$$\overline{v_{n,out}^2} = \frac{g_{m7}^2 (R_f \,//\, r_{o9})^2 a^2}{(1+\frac{a g_{m3} g_{m7}}{g_{m5}})^2} \overline{i_n^2} \tag{9}$$

where, $a = (\frac{g_{m5} r_{o11}}{g_{m5}+g_{m7}})(\frac{g_{m1} R_s}{1+g_{m1} R_s})$ and, $\overline{i_n^2} = \overline{i_{n,M3}^2} + \overline{i_{n,R_s}^2}$ ; $g_{mi}$ and $r_{oi}$ are transconductance and output resistance of the transistor $M_i$.

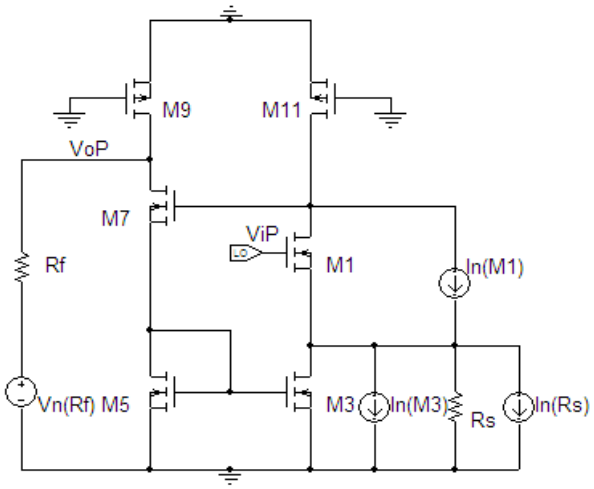


**Fig. 4.** Calculation of the input-referred noise of the proposed VGA-cell

Referring to the input port, $\overline{v_{\mathrm{n,in}}^2} = \dfrac{\overline{v_{n,out}^2}}{|A_{Vo}|^2}$, the input referred noise due to $M_{3,4}$ and $R_s$ can be approximately expressed as:

$$\overline{v_{n,in}^2} = \left( \frac{1}{1+\dfrac{g_{m7}}{g_{m5}}} \right)^2 \left( \frac{g_{m1}R_S}{1+g_{m1}R_S} \right)^2 R_S^2 \overline{i_n^2} \qquad (10)$$

The noise due to input transistor $M_1$ and resistance $R_f$ can be added to estimate the total input-referred noise as,

$$\overline{v_{n,in(tot)}^2} = \frac{1}{g_{m1}^2}\overline{i_{n1}^2} + \left( \overline{v_{n,R_f}^2} + \overline{v_{n,out}^2} \right) \left| \frac{1}{A_{V0}} \right|^2 \qquad (11)$$

where, $\overline{i_{n,M_i}^2} = 4kT\left(\frac{2}{3}g_{mi}\right)\Delta f + K\frac{I_{Di}^a}{f}\Delta f$ , $\overline{i_{n,R_s}^2} = \frac{4kT}{R_S}\Delta f$ , and $\overline{v_{n,R_f}^2} = 4kTR_f\Delta f$ .

At low-gain settings, $A_{v0}$ becomes small and so the last term in (11), defined by (10), dominates the noise performance of the circuit. As a result, $R_S$ should be chosen small enough for good noise performance. In contrast, at large-gain settings, noise performance

is dominated by the first term in (11) (input transistors $M_1$ and $M_2$) and consequently $g_{m1}$ should be maximized.

### *2.3. Output CMOS Buffer*

Our proposed buffer circuit [10] is shown in **Fig. 5**. The circuit has achieved large transconductance without increasing the aspect ratio of the main differential transistors $M_1$ and $M_2$. The basic idea of the buffer is to improve the bandwidth based on the Flipped Voltage Follower (FVF) by enhancing the transconductance of $M_3$ ($M_4$) through the feedback loop $M_1$, $M_7$, and $M_5$ ($M_2$, $M_8$, and $M_6$).

The circuit is biased by two pairs of current sources ($M_9$ and $M_{10}$) and ($M_{11}$ and $M_{12}$); the former pair supplies low current to the main differential transistors, and so small loading-effect is observed at the input of the buffer. The latter pair is used to enhance the required current needed for driving large capacitive load. The feedback is accomplished through the level shifter $M_5$ and $M_7$ ($M_6$ and $M_8$) to increase the swing headroom for $M_1$ ($M_2$), and consequently the linearity.

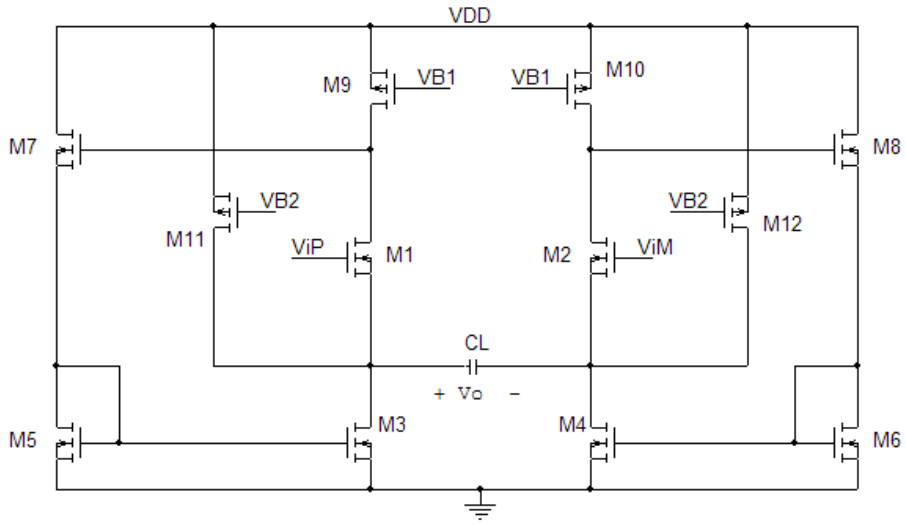


**Fig. 5.** Proposed buffer circuit [10]

The output voltage ($V_{oP}$) half-circuit of the small-signal model is shown in **Fig. 6** (half of the circuit is shown for clarity). One-half of the circuit is only considered for simplicity without loss of generality.

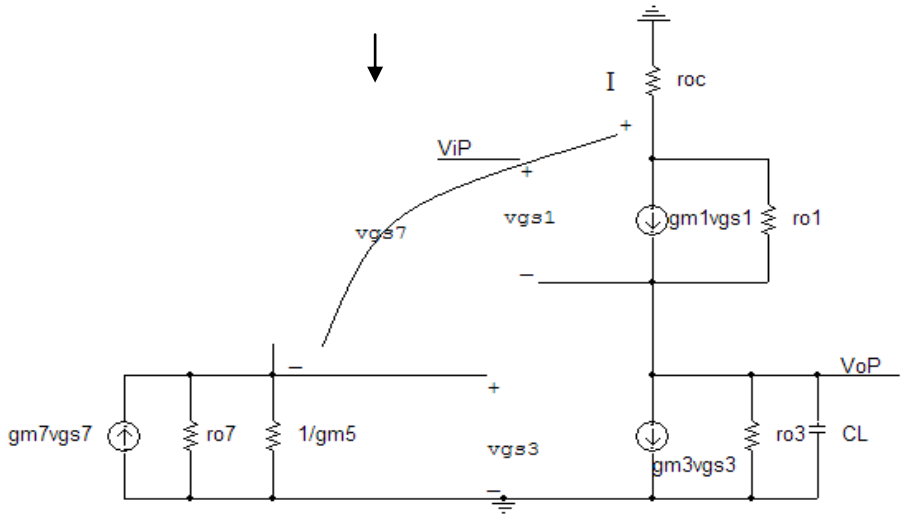


**Fig. 6.** Small-signal model of the proposed buffer

A similar analysis, to what has been done in Section II.A, can be conducted to calculate the output voltage gain $A_V$,

$$A_v = \frac{A_O}{1 + j\omega \dfrac{C_L}{g_{meff}} A_O} \qquad (12)$$

Where $A_o$ is the DC gain defined by,

$$A_0 = \left[ \frac{\dfrac{g_{m1} r_{o1} r_{o3} \left[1 + (g_{m5} + g_{m7}) r_{o7} + g_{m3} g_{m7} r_{o7} r_{oc}\right]}{(r_{o1} + r_{o3} + r_{oc})\left[1 + (g_{m5} + g_{m7}) r_{o7}\right] + g_{m3} r_{o3} g_{m7} r_{o7} r_{oc}}}{1 + \dfrac{g_{m1} r_{o1} r_{o3} \left[1 + (g_{m5} + g_{m7}) r_{o7} + g_{m3} g_{m7} r_{o7} r_{oc}\right]}{(r_{o1} + r_{o3} + r_{oc})\left[1 + (g_{m5} + g_{m7}) r_{o7}\right] + g_{m3} r_{o3} g_{m7} r_{o7} r_{oc}}} \right] \qquad (13)$$

and

$$g_{meff} = \left[ \frac{g_{m1} r_{o1} r_{o3} \left[1 + (g_{m5} + g_{m7}) r_{o7} + g_{m3} g_{m7} r_{o7} r_{oc}\right]}{r_{o3} (r_{o1} + r_{oc})\left[1 + (g_{m5} + g_{m7}) r_{o7}\right]} \right] \qquad (14)$$

If $r_{oc}$, $r_{o1}$ and $r_{o7}$ are very large and the term $r_{o3}g_{m3}$ is much greater than unity, the effective transconductance can be reduced to,

$$g_{meff} = g_{m1}\left[1+\frac{g_{m3}g_{m7}r_{oc}}{(g_{m5}+g_{m7})}\right] \qquad (15)$$

From (15), the overall transconductance is approximately improved by the closed loop gain from input to the ac current of $M_3$-$M_4$, through ($M_1$, $M_7$, $M_5$, and $M_3$), which is very large. The overall transconductance was improved by a factor proportional to approximately $g_m r_{oc}$ without increasing the basic transistor size. On the other hand, the THD is superior for our proposed cell compared to the FVF cell.

## 3. VGA implementation and simulation results

### *3.1. Variable gain amplifier*

The VGA is implemented in 0.13-µm IBM CMOS process. The design equations, derived in the previous section, are used to guide our design. The VGA achieves the required bandwidth of 400 MHz with gain varying from -0.5 dB to 54 dB using 5-bits control-word. It consists of three identical VGA-cells. $R_s$ is used to generate coarse-gain steps of 16 dB each whereas $R_f$ is used to generate fine-gain steps of 2 dB each. Compensation capacitor array $C_s$ has been also used in parallel with $R_s$ to introduce a programmable zero into the transfer function that can be employed to widen out the bandwidth at large gain settings. The overall simulated variable gain amplifier current dissipation is 21 mA.

**Fig. 7** shows the gain plot versus gain-control word for the simulated and analytical results equation (6); the gain is clearly linear-in-dB. There is also good agreement between analytical and simulated plots across wide gain dynamic range from -0.5 dB up to 54 dB. The insensitivity to process variation has been also studied, where there are only 0.5 dB deviations from the results of the typical mean process parameters.

**Fig. 8** shows the frequency response for different gain settings. The bandwidth decreases as the gain increases, however bandwidth could be kept at its minimum value of 400 MHz by controlling the zero location without significant increase in power consumption. While the bandwidth at the maximum gain can achieve 400 MHz, the bandwidth at the minimum gain extends to 2 GHz. It is also worthy to mention that the peak occurs outside the bandwidth of interest.

The linearity performance of VGA is characterized by two-tone IIP3 test. It was measured by applying two tones of 100MHz and 120MHz at the lowest gain mode. The result is shown in **Fig. 9** where IIP3 is equal to17.6dBm. **Table 1** compares our work against others' work in the literature. The GBW/power is taken as a figure of merit for a reasonable comparison. Our VGA shows the highest figure-of-merit. The circuit also

shows reasonable noise performance, which can be certainly improved at the expense of higher power consumption.

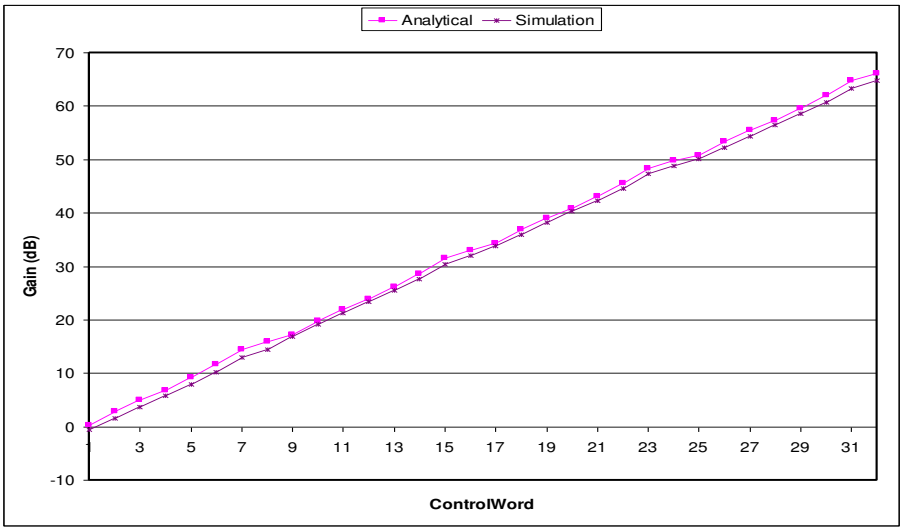


**Fig. 7.** Linear-in-dB gain versus control word

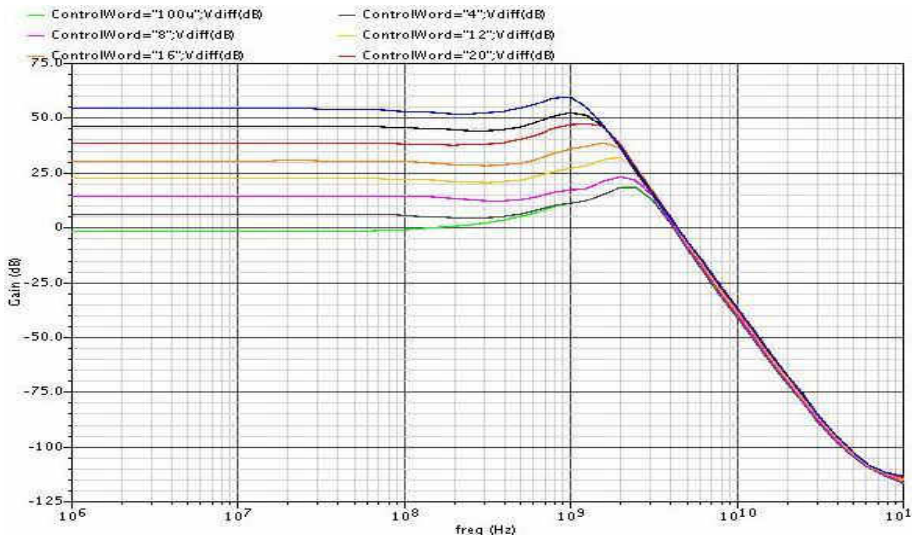


**Fig. 8.** Gain versus frequency for different gain settings

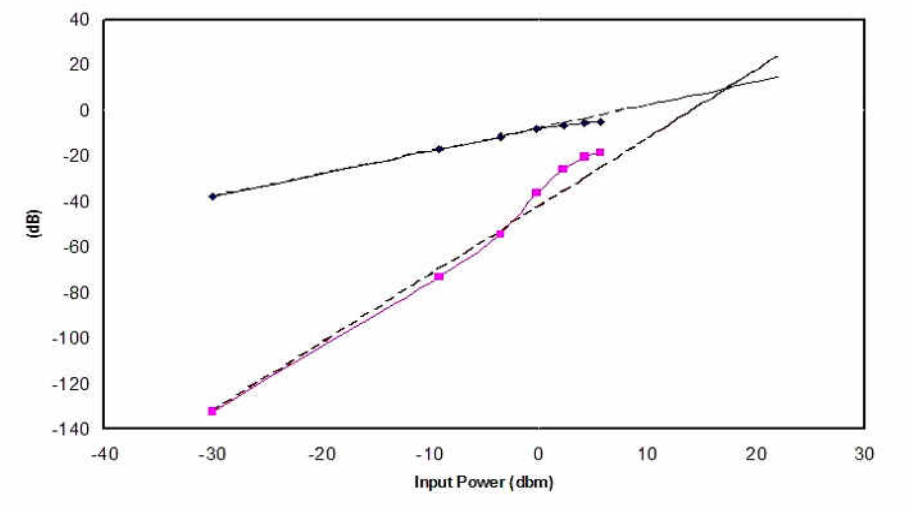


**Fig. 9.** The IIP3 at the lowest gain mode

**Table 1**
Performance summary and comparison

| Parameters | [17] | [18] | [19] | [20] | This Work |
|---|---|---|---|---|---|
| Technology | 0.18µm | 0.18µm | 0.18µm | 0.13µm | 0.13µm |
| Supply voltage | 1.8V | 1.8V | 1.8V | 1.5V | 1.5V |
| Bandwidth (MHz) | 450 | 650 | 400 @54dB | 183 – 548 | 1500 |
| Gain range | 3 – 47 dB | 0.7 – 60.7dB | -30 – 65 dB | -5 – 65 dB | -0.5 – 54 dB |
| IIP3 | 20dBm | | | | 17.6 dBm |
| Current dissipation | 15mA | 8.9mA | 12.2mA | 13.4mA | 21mA |
| $P_{diss}$ (mW) | 27 | 16.02 | 21.96 | 20.1 | 31.5 |
| THD @ freq=400MHz & $V_{od(p-p)}$=1 V | | | | | -49.47 dB @ 54 dB<br>-43.26 dB @ -0.5 dB |
| Input referred noise | | | | | 121.6 nV/√Hz @ -0.5 Db |

| Parameters | [17] | [18] | [19] | [20] | This Work |
|---|---|---|---|---|---|
| GBW/Power(MHz/mW) | 7518 | 48507 | 53083 | 48438 | 56103 |

### *3.2. The overall VGA*

**Table 2** summarizes the crucial simulation results of the overall variable gain amplifier with the output buffer at maximum and minimum gain settings. The buffer is loaded with a capacitive single-ended load of 2 pF. The noise performance of the circuit is dominated by the VGA, Table 2; the buffer noise is insignificant because of its large transconductances and so small input referred noise.

**Table 2**
Summary of the simulation results of the overall VGA

| Parameters | @ -0.5 dB | @ 54 dB |
|---|---|---|
| Bandwidth (GHz) | 3.5 | 1.5 |
| Average Integrated Noise (nV/√Hz) | 121.6 | 17.4 |
| THD (dB) @ 400 MHz and $V_{odp-p}$=1 V. | -40.04 | -42.31 |
| Power dissipation (mw) | 37.5 | |

**Fig. 10** shows the frequency response of the overall VGA at the extreme gain settings. As seen from **Fig. 10,** the frequency response extends for more than 400 MHz. Although the small-signal bandwidth can be as large as 1.5 GHz, the effective bandwidth is limited to 400 MHz only, for output voltage swing of 1 $V_{dpp}$ with the aforementioned loading, owing to the slew-rate limitation.

## 4. Conclusions

This paper presents a low-voltage CMOS VGA. It achieved wide bandwidth over wide dynamic gain range from -0.5 dB to 54 dB. With this circuit topology, the gain and bandwidth can be programmed independently. The circuit has been designed and implemented using 0.13 μm IBM-CMOS process with supply voltage of 1.5 V and power dissipation of 37.5 mW to drive 2 pF single-ended capacitive loads.

This VGA can be applied to various applications, such as high performance industrial systems and baseband circuits in multi-standard wireline and wireless communications with wide bandwidth.

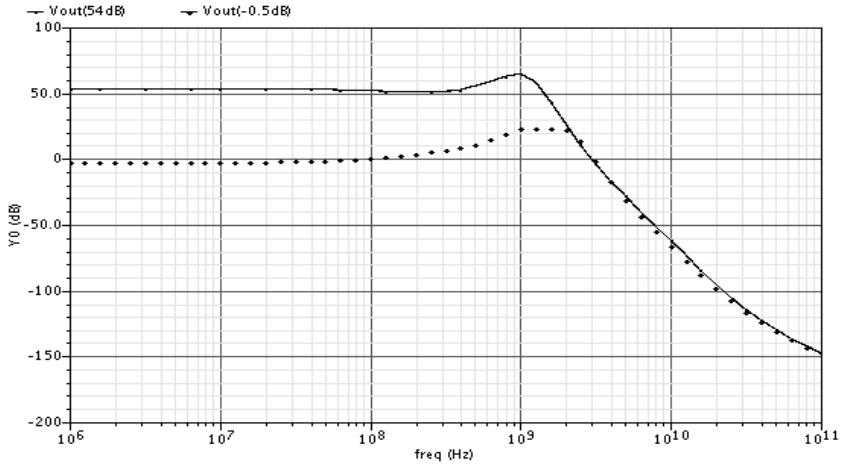


**Fig. 10.** Frequency response for the overall VGA

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# مكبر جهد (CMOS) ذو عامل كسب متغير لتطبيقات النطاق الترددي الواسع (UWB) عالي الخطية

**ملخص:**

- البحث يقدم مكبرجهد ذو عامل كسب متغير ***(VGA)*** للاستخدام في التطبيقات ذات النطاق الترددي الواسع. الدائرة الالكترونية المقدمة تمتازبارتفاع قيمة سعة الجهد في المرحلة الخطية. المكبر المقترح يتركب من ثلاث مراحل متعاقبة من ***VGA*** مع وجود مرحلة عزل ***Buffer*** كوحدة خرج. الدائرة المقترحة – بهذه الموصفات- تصبح مناسبه للاستخدام في بروتوكولات الاتصالات القياسية والتي تحتاج الي حيز ترددي واسع. عند تصميم الدائرة المقترحة تم استخدام بعض الطرق لتقليل الطاقة المستهلكة كما تم تقديم وتحليل نموذج الشوشره الذاتية الناتجه من هذا المكبر. الدائرة المقدمة تم تصميمها ومحاكاتها علي الحاسب وذلك باستخدام تكنولوجيا الـ ***CMOS*** و المقدمة من شركة ***IBM*** ذات الابعاد 0,13 ميكرو . النتائج اظهرت ان الدائرة المقترحة في هذا البحث تحقق تحسن في كثير من عوامل القياس المتبعة في الدوائر المتكاملة التناظرية وعلي سبيل المثال فهي تحقق: أتساع نطاق الدخل ***DR=54.5dB*** و ***IIP3=17.6dBm*** و***THD=-42.3dB*** وذلك عند جهد دخل 1,0 ***V*** من القمة للقمة وتردد يساوي (400 مجاهرتز). وعلاوة علي ذلك فأن الدائرة ***(VGA)*** أظهرت مشاركة قليلة بالنسبة لمتوسط الشوشرة الناتج عن الدائرة عند اقل معامل كسب(***-0.5dB***) معمل الشوشره كان ***121.6 nV/√Hz***.