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AVERAGE CURRENT CONTROL FOR AIRCRAFT APPLICATIONS

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Five, single-phase H-bridge converters are used to interface variable-speed, permanent magnet generator into a common DC bus. To draw high quality current from the generator and provide constant DC voltage, a modified implementation of the average current control technique is proposed. A phase shift circuit was added to the average current control to allow system operation at different load and speed conditions. The proposed technique has a significantly fast dynamic performance. The analysis was validated using rigorous simulation.

1- INTRODUCTION

Recently, the aerospace industry adopts electrical power as a primary source for extracting and distributing non propulsive powers of air vehicles. This trend is themed More-Electric Aircraft (MEA) [1-2]. The embracing of MEA, as claimed in [1-2], radically change the aerospace industry, and significant improvements in terms of aircraft-empty weight, reconfigureability, fuel consumption, overall cost, maintainability, supportability, and system reliability would be realized. However, MEA increases the demands on the aircraft electric power system in areas of power generation, handling, reliability, and fault tolerance, which mandates innovations in power generation, processing, distribution and management systems [1-2].

A five-phase, permanent magnet, fault-tolerant generator is proposed to be coupled with the aero-engine low pressure shaft [3-4] to meet the increased demand of on-board electric power. The generator phases are physically, magnetically, thermally and electrically isolated. The generator utilizes the windmilling effect of the low pressure shaft to generate electrical power during emergency conditions such as engine failure. Five single-phase PWM H-bridge converters are used to interface the generator terminals into a common DC bus [3-4]. To minimize the generator copper losses, the generator phase current has to be in phase with the emf at low-medium speeds, mode 1, and lags the emf at high speeds, mode 2 [3-4]. A simple and efficient control technique for the system is proposed in [3-4]. However, this technique produces large deviation in the DC voltage during transient conditions. Moreover, this scheme has slow dynamic response.

Average Current Mode (ACC) control [5-8] enables very accurate tracking of the sinusoidal reference and results in low harmonic distortion in the AC output. This technique, as claimed in [5-6], has high noise immunity. Furthermore, numerous, low cost, dedicated integrated circuits are available for its implementation. However, the technique in its basic form is only suitable for constant speed operation [5-8]. Therefore, an innovative implementation of the ACC is required to allow its

application for areas such low pressure shaft generator, where there is wide speed\frequency range.

In this paper a modification of the ACC is proposed for applications where speed/frequency varies widely. A detailed design for the controllers is given, and the analysis has been validated using rigorous simulation work in Saber environment.

2- SYSTEM DESCRIPTION AND CONTROL DESIGN

An Individual H-bridge converter is attached to each generator phase as shown in Fig. 1 to comply with the fault-tolerance strategy of the generator system

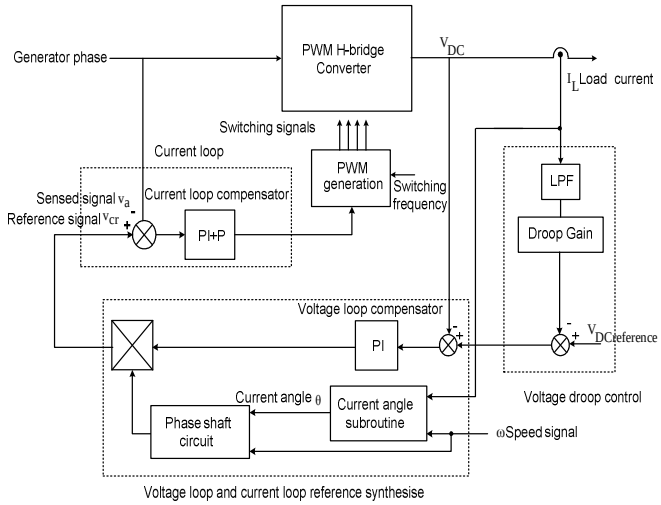

Fig 1: Schematic diagram of single phase PWM H-bridge converter and the proposed ACC

In the proposed ACC as shown in Fig. 1, current angle algorithm and phase shift circuit are employed to adjust the angle of the reference with respect to the generated voltage according to the generator speed and load conditions.

In the current loop of the proposed ACC, the converter current is sensed through a voltage drop va across a resistor. The sensed signal va is compared with the reference signal vcr and the error is applied to PI plus pole compensator. The output of the compensator is supplied to a PWM generation block. The amplitude of the reference signal vcr is set by the voltage loop so that the converter input power instantaneously matches the load power. The division of the reference signal by the square of the source voltage RMS used in [5-8] is removed in the proposed ACC as this circuit is a source of failure in the control circuit. Moreover, it complicates the design process of the compensators in the conventional ACC. The design of the modified ACC loops shown in Fig.1 is discussed in detail in the following.

The voltage droop control shown in Fig. 1 is used to ensure equal load sharing among the five generator/converter modules. The parameters of the system under concern are given in Table 1.

Table 1: The parameters of the system under concern [3,4]

Rated power	70kW
Number of phases	5
Speed range	1000-3000rpm
EMF(RMS)	160V at 1000rpm
RMS rated current	87.5A
Per-phase inductance	1.3mH
Per-phase resistance	46m Ω
Phase separation	72^0
Output DC voltage	540VDC
Pole-pair	14

2.1 Current Loop

The schematic diagram of a single-phase H-bridge and the current loop of the proposed ACC are shown in Fig. 2

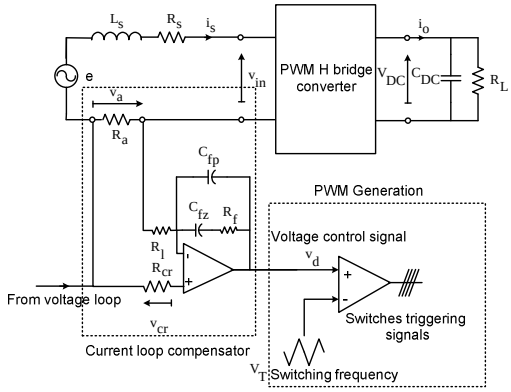

Fig. 2: Schematic diagram of the single phase PWM H-bridge converter and the inner loop of the proposed ACC

In Fig. 2, Ra, Rl, Rcr, Rf, Cfp and Cfz are the elements of the current loop compensator. VT is peak-to-peak of the triangle switching signal, and vd is the voltage control signal.
The values of Ra , Rl, VT and switching frequency fs are given in Table 2.

Table 2: Parameters of current loop in the proposed ACC

f_s (kHz)	R_a (Ω)	R_l (kΩ)	VT (V)
100	0.1	10	20

The resistor Ra shown in Fig. 2 is not directly embedded in the path of the current, but connected to the secondary of 1:100 current transformer. This is to provide dielectric isolation and reduce the power loss.

In the design of the current loop, the voltage loop is assumed to be relatively slow. Therefore, the system can be assumed single-pole system.

To prevent instability at switching frequency, the current loop gain Gc=Rf/Rl is determined by [5],

$$G_c = \frac{V_T f_s L_s}{V_{DC} R_a} \tag{1}$$

The current loop gain for the system under concern is 48; therefore the resistor Rf is 0.48MΩ. With the current loop gain set to its maximum value, (1), the current loop cross over is at 16.7kHz. The zero Rf* Cfz is set at half of the current loop cross over frequency to provide boost for the low frequency gain. Accordingly Cfz is 250nF.

The pole Rf *Cfp*Cfz/(Cfp +Cfz) is set at half of the switching frequency to eliminate the switching frequency ripple. Accordingly Cfp is 50nF.

2.2 Voltage Loop

To simplify the design of the voltage loop in the proposed ACC, the following assumptions were used:

- The DC-link voltage V_{DC} is assumed constant.
- The machine/converters system is assumed lossless.

These assumptions results in equal instantaneous input and output power of the converter module,

$$ei_S = i_o V_{DC} \tag{2}$$

When the current loop is closed, the following relation is satisfied [5]

$$i_S = \frac{v_{cr}}{R_{cr}} \tag{3}$$

The converter output current io, Fig. 2, is given by,

$$i_o = C_{DC} \frac{dV_{DC}}{dt} + \frac{V_{DC}}{R_L} \tag{4}$$

Equations (2)-(4) are linearized by applying the steady-state averaging technique [9]. In this technique, the state variables VDC and vcr are perturbed around a steady-state operating point as follows,

$$v_{cr} = \left| v_{cr} \right|_o + \Delta v_{cr} \tag{5}$$

$$V_{DC} = V_{DCo} + \Delta V_{DC} \tag{6}$$

Where steady state operating points are represented by the variables with the subscript ‘o’, while ‘ Δ ’ before a variable denotes a small signal variable.

Substituting (5)-(6) into (2)-(4) and multiplying out and neglecting products of small-signal terms, then separating the steady-state parts from the small-signal terms results in the first order terms as:

$$\frac{E\Delta v_{cr}}{R_{cr}} = V_{DCo}\left(C_{DC}\frac{d\Delta V_{DC}}{dt} + \frac{2\Delta V_{DC}}{R_L}\right) \tag{7}$$

Applying Laplace transform to (7) gives the transfer function between Δv_{cr} and the DC-link voltage ΔV_{DC},

$$\frac{\Delta V_{DC}}{\Delta v_{cr}} = G_a(s) = \left(\frac{E}{V_{DCo}C_{DC}R_{cr}}\right)\left(\frac{1}{s+\frac{2}{R_L C_{DC}}}\right) \tag{8}$$

The converter and the current loop are represented by a single pole transfer function (8). This pole results from the interaction between the load resistance RL and the DC filter capacitor CDC.

A PI compensator Ca(s) was used in the voltage loop to regulate the DC voltage VDC. The block diagram of the voltage loop in the modified ACC is shown in Fig. 3.

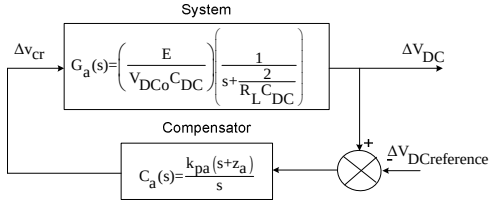

Fig. 3: Block diagram of the voltage loop in the proposed ACC

In order to increase the bandwidth of the voltage loop, the compensator zero za is placed at the same frequency as the pole of the converter open loop transfer function Ga(s). However, the bandwidth of the voltage loop should be chosen such that an adequate damping for the second harmonic ripple in the converter DC voltage VDC is provided without adversely affecting the stability margin. It was found for modified ACC operating in the speed range from 500-3000 rpm that a bandwidth of 200 rad/sec is a good compromise between the second harmonic attenuation and the response speed. Accordingly, the compensator gain kpa has been chosen. The parameters of the compensator in the voltage loop are given in Table 3.

Table 3: Parameters of the voltage loop compensator in the modified ACC

za rad/sec)	kpa
125	0.2

The frequency performance of the transfer function ΔVDC/ΔVDCreference was investigated at different operating points of load and speed, the bandwidth and the phase margin are given in Table4.

Table 4: Frequency response of ΔVDC/ΔVDCreference at different speed and load levels

Load resistance (Ω)	500rpm		2500rpm	
	Band width (rad/sec)	Phase margin (degree)	Band width (rad/sec)	Phase margin (degree)
20	**200**	**90**	1021	90
24	212.2	86.5	1028	89.5
120	240.8	63.9	1060	65

Table 4 shows that the bandwidth increases with the speed; therefore the system dynamic response at high speeds is faster than that at low-medium speeds. The phase margin decreases with the load reduction; however the minimum value of phase margin 63.9o at 500rpm and 120 Ω load is acceptable.

2.3 Phase Shift Circuit

The principle target of the phase shift circuit as mentioned before is to adjust the angle of the reference current according to load and speed conditions.

The angle θ calculation algorithm is shown in Fig. 4. In order to simplify the calculation, the assumptions stated above in the voltage loop design are applied.

The algorithm starts by reading the constants: DC-link voltage VDC, per-phase inductance Ls, minimum speed ωo and the minimum emf Emin. The constant of the generated voltage is calculated by,

$$k_e = \frac{E_{min}}{\omega_o} \tag{9}$$

Then, the algorithm reads the actual speed ω and the load current IL. The load power P is the product of the load current IL and DC voltage VDC. The boundary speed ωb between the low-medium speed range and the high speed range is calculated by,

$$\omega_b = \frac{1}{k_e}\sqrt{V_{DC}^2 - \left(\frac{PL_s}{k_e}\right)^2} \tag{10}$$

The angle θ is calculated according to the comparison of ω and ωb. For example, if $\omega \le \omega b$, the angle θ is set to zero, otherwise it is calculated by,

$$\theta = \tan^{-1}\left(\frac{P}{Q}\right) \tag{11}$$

where P and Q are active and reactive powers respectively.

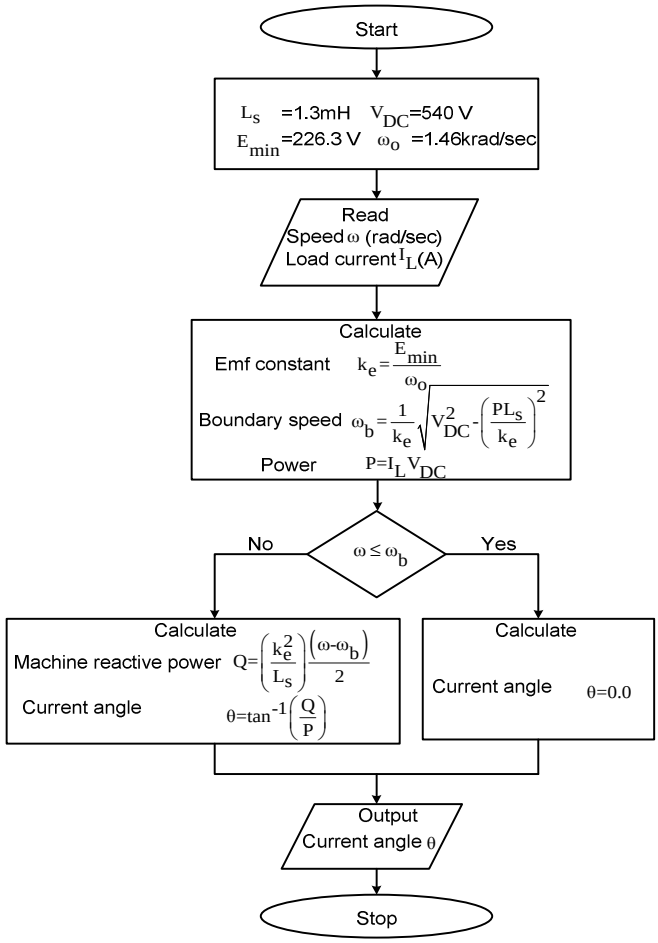

Fig. 4: Schematic diagram of the current angle θ algorithm

3- RESULTS AND DISCUSSION

Two programs are developed in Saber environment to validate the analysis. The first program stimulates the averaged-value model [4] of the system depicted in Fig. 1, while the second one represents the switched model of the H-bridge converter. However, the switches in the switched model are assumed ideal.

The DC-link voltage VDC, current angle θ, current and supply voltage obtained from simulation programs are shown in Figures 4-6 for a step change in load from 120Ω (2.4kW) to 24Ω (12.1kW) at 1.9 sec and from 24Ω to 120Ω at 1.97sec and speed of 2200rpm.

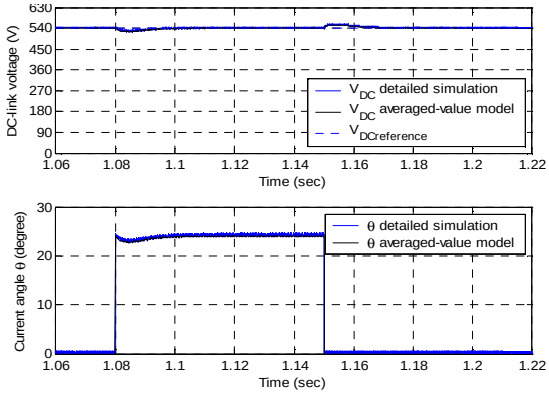

Fig. 4: DC voltage V_{DC} (top), angle θ (bottom) from switched simulation (blue) and averaged-value model (black) for a load step of 120Ω to 24Ω at 1.9 sec and step of 24Ω to 120Ω at 1.97sec and speed of 2200rpm

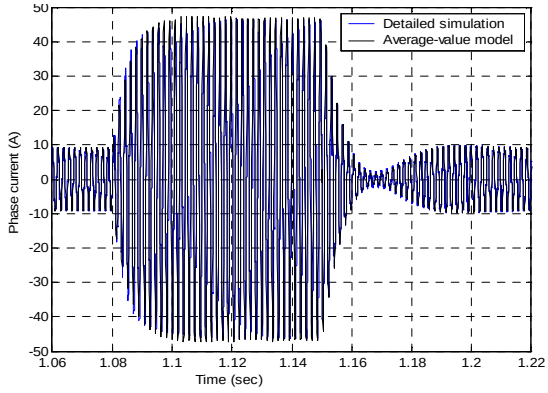

Fig 5: Phase current from switched simulation (blue) and averaged-value model (black) for a load step of 120Ω to 24Ω at 1.9 sec and step of 24Ω to 120Ω at 1.97sec and speed of 2200rpm..

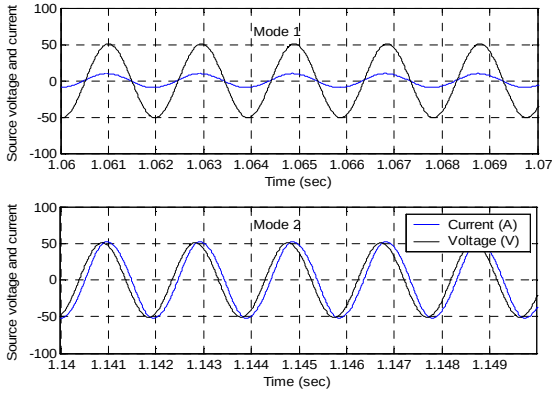

Fig 6. Supply voltage/10 (black) and current (blue), top graph for 120Ω load (mode 1), bottom graph for 24Ω load (mode 2) at speed of 2200rpm.

In general, there is a good corroboration between detailed and average models the result shown in Figures 4-6.

The system initially operates in mode 1 at low load (2.4kW), where the current is in phase with the supply voltage, Fig. 6. For high load, 12.1kW, the operating point moves to mode 2 [3], where the current lags the supply voltage. The smooth transfer from between the different modes is attributed to the phase shift circuit.

The deviation in DC-link voltage for step change from no-load to full load condition at 2200rpm is around 2.7%, Fig. 4. The system requires only 20msec to settle down for full load step change. The system dynamic response was investigated at different speeds and load conditions, and it was found that largest deviation in the DC-link voltage occurs at 1000rpm and 20Ω operating point is only 5.5% of the DC-link voltage.

Comparing the proposed ACC with the voltage vector control [3,4] indicates that the proposed technique has significantly faster dynamic response with lower DC-link voltage deviation during load transients. However, the voltage vector control has albeit high efficiency due to reduced switching losses [4].

4- CONCLUSION

A modified implementation of the ACC is proposed for five-phase, permanent magnet generator in aircraft applications. A phase shift circuit was used to comply with the generator variable speed operation. The circuit adjusts the reference current in such way to optimize the generator copper losses.

Detailed design for the controller loops was carried out. The zero of the current loop is placed at half the cross-over frequency to increase the loop low frequency gain, while providing around 45o phase margin at cross over frequency. The pole of the current loop is allocated at half the switching frequency to attenuate switching frequency ripple.

In the voltage loop a PI controller is used, the parameters of the controller are selected to provide adequate bandwidth of 200rad/sec at low frequency, while maintaining system stability.

The system was found to have faster dynamic response in the medium-high speed range.

The proposed ACC utilizes a high switching frequency to ensure reference current tracking; however this increases the power loss and hence decreases the efficiency.

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متوسط التيار لمولد

يقدم هذا البحث معالجة جديدة لطريقة متوسط التيار لمولد مقاوم للأخطاء ذو خمس أوجة . النتائج تم التاكد منها عن طريقة المحاكاة .