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NOVEL SOFT SWITCHING TECHNIQUE OF SYNCHRONOUS BUCK CONVERTER BASED ON ZVS-QSW WITH ADAPTIVE TECHNIQUE

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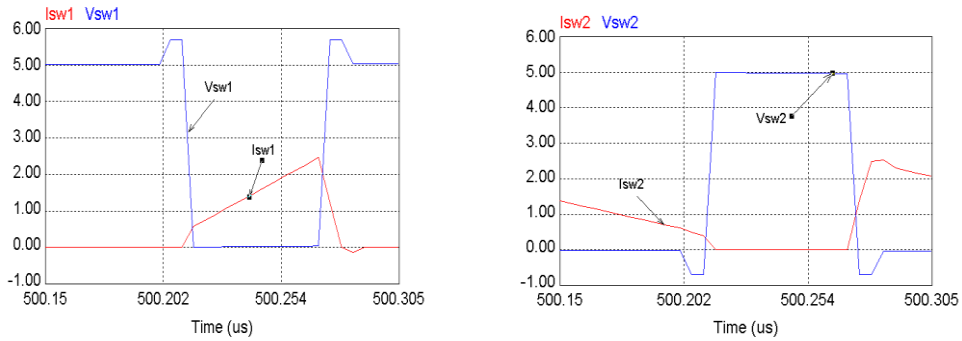
Nowadays, the main important issue for power supplies designers is to feed last generation of microprocessors and DSPs, since they require high current slew rates on accompain with low output voltage. The most important issue with these power supplies is the efficiency, especially with ultra-high switching frequency. The main factor of limitation for these target systems with ultra-high switching frequency is the switching losses and body-diode losses. Zero-Voltage-Switching Quasi-Square-Waveform (ZVS-QSW) has been proposed to solve the matter of switching losses; however, it can not achieve that for wide-load applications. Besides, adaptive technique has been introduced to reduce the body-diode losses. In this paper, in this paper the advantage of the two techniques is assumed by merging them together. Moreover, a modification circuit is proposed to apply soft-switching technique for the main switch. In conclusion, novel soft switching technique is proposed for high-switching frequency synchronous buck converter based on ZVS_QSW and adaptive technique. The mathematical model is introduced and confirmed using PSIM simulation using 5MHz synchronous model.

I. INTRODUCTION

Research has been developed in order to reduce weight and size of the switching converters to achieve the technological advance which demands equipment with high-power density. High-switching frequency operation is a way to obtain converters with those characteristics. However, the increasing of switching frequency results in an increase of switching losses body-diode losses and gate-drive losses. Consequently, this decreases the efficiency of the conventional Pulse Width Modulation (PWM) switch mode converters. Moreover, many portable devices operate in low-power standby modes for a majority of the time that are on then Increasing light-load converter efficiency can significantly increase battery lifetime. Therefore, increasing converter efficiency over all load range becomes the challenge.

When the conversion frequency of conventional PWM supplies approaches 1MHz the switching losses becomes excessive due to the simultaneous presence of a high current and high voltage during turn-on and turn-off [1] as shown in Fig.1. Figure 1 explains the simulation of 5MHz synchronous buck converter for 5/1.5V-1.5A. Synchronous rectification allows to reduce power losses in low voltage converters, but

as the switching frequency is increased the switching loss, the gate drive loss and the body diode loss increase, vanishing the advantages of the synchronous rectifier. First, the main cause of switching losses is the current voltage overlap[1]. The current-voltage overlap losses are caused by the gate capacitors this clarify that the dominant switching losses occurs at the main (active) switch. Synchronous switch is already has soft switching through its body diode. Second, as the dead time increases, the body diode losses increase. Moreover, the switch turn-on at high voltage creates high switching losses.



(a) The current and voltage of switch 1 b) The current and voltage of switch 2

Fig.1 The current and voltage of synchronous buck converter at hard switching.

II. SOFT SWITCHING TECHNIQUES

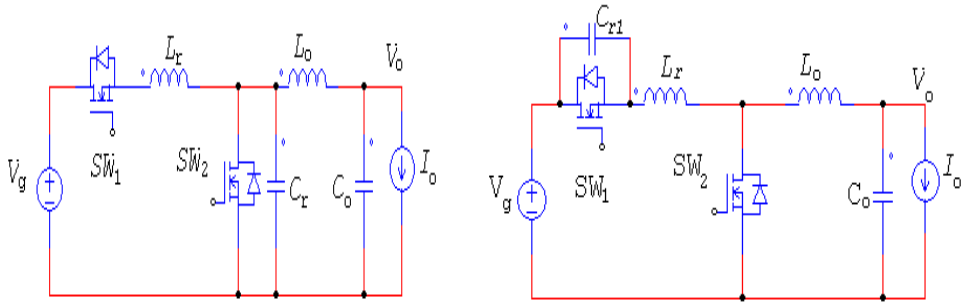
Reducing losses is one of the important aims in low voltage DC-DC converter application. One of these losses is the switching losses which can be reduced by several approaches to obtain soft switching. It is preferable to reduce the voltage on the switch to be zero or near zero at their turn-on transition to operate MOSFETs with zero voltage switching at their turn-on transitions or reduce the current of the switch to be zero or near zero at their turn-off transition to operate MOSFETs with zero current switching at their turn-off transitions. However, zero-voltage switching or zero current switching comes at expense of increased conduction loss, so the effect of soft switching on the overall converter efficiency must be considered [2].

Obtaining zero-voltage or zero-current switching requires the resonant element to have large ripple; often, these elements are operated in a manner similar to the discontinuous conduction modes of the series of parallel resonant converters as in resonant schemes, the objectives of designing such converter are[3]:

1- To obtain smaller transformer and low-pass filter elements via the increase of the switching frequency.
2- To reduce the switching losses induced by non-ideal components such as semiconductor device, capacitances, transformer leakage inductance and winding capacitance.

Electronic power processing technology has evolved around two fundamentally different circuit schemes: duty cycle modulation, commonly known as Pulse-Width Modulation (PWM), and resonance. The PWM technique processes power by interrupting the power flow and controlling the duty cycle, thus, resulting in

pulsating current and voltage. The resonant technique processes power in a sinusoidal form. The power switches are often commutated under zero-current ("soft" turn-off) but switches are turned on with an abrupt increase of device current. In cases where resonant converters operate above the resonant frequency, the switches are turned off abruptly (forced or hard turn-off) but turned on softly. Fig. 2 shows the circuit of ZCS and ZVS. Compared with PWM converters, the switching losses and stresses of resonant converters are reduced; however, the conduction loss is generally increased since the sinusoidal current produces higher RMS current [4]. Due to circuit simplicity and ease of control, the PWM technique has been used predominantly in today's power electronics industry, particularly, in low-power applications. Resonant technology, although well-established in high-power motor drives and uninterrupted power supplies, has not been widely used in low power DC-DC converter applications due to its circuit complexity [5-7].



a) ZCS technique b) ZVS technique

Fig. 2 Quasi resonant synchronous buck converter circuits.

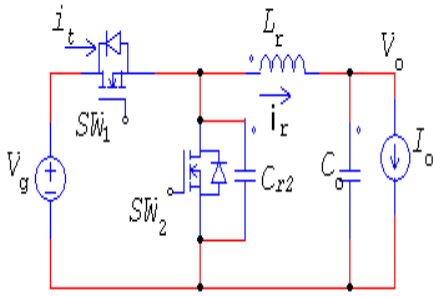


Fig. 3 Zero-voltage quasi square

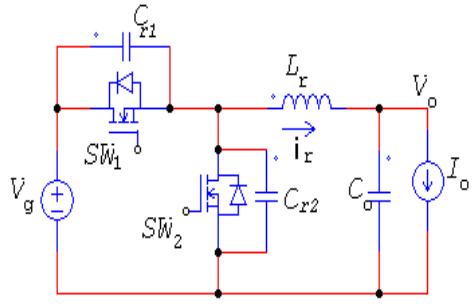


Fig. 4 Modification topology of ZVS-QSW

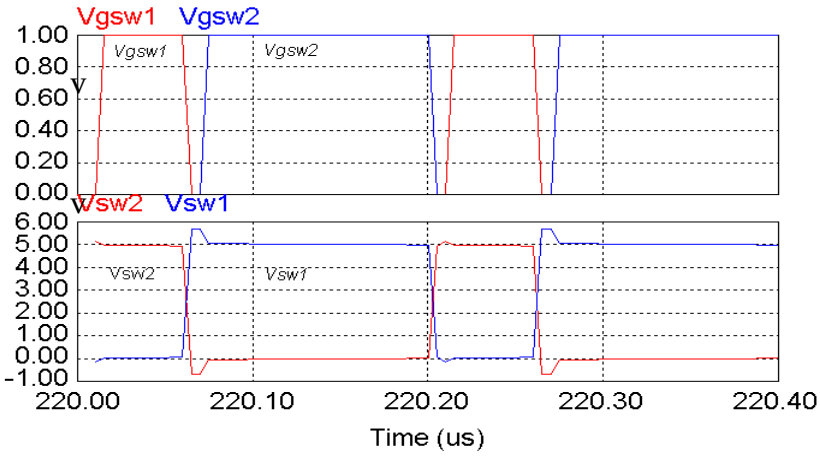


Fig. 5 Wave form of ZVS-QSW at 5 MHz at full load.

III. QUASI-SQUARE CONVERTERS

Quasi resonant converters with zero current have high current stresses and low voltage stresses. On the other hand, the zero voltage switching has lower current stresses but higher voltage stresses. The solution of this problem is quasi square topologies [8]. Reducing the output inductance L_r of a synchronous buck converter beyond a critical value will result in discontinuous operation. However, continuous inductor current is achieved using bi-directional power switches, resulting in quasi-square-wave (QSW) operation as shown in Fig. 3, where C_r is the resonant capacitor that incorporates the output capacitances of the MOSFETs.

By this technique a lot of benefits can be achieved:-

1- Less voltage stress, this is a very desirable feature for high frequency conversion since the MOSFETs have low resistance.
2- Bidirectional power flow
3- Small size (small inductance and less components as comparative of quasi resonant converter)

But in the other hand there are two disadvantages:-

1- High current stress in comparative of PWM converter.
2- Large inductor current ripple (small inductance, small inductor resistance) that increases the conduction losses.

One of the drawbacks of previous topology is the conduction of the body diode, so a second resonant capacitor is connected in parallel with active switch (SW_1) as shown in Fig. 4., the positive charge on C_{r1} prevents the body diode of the main switch (SW_1) to conduct, this way forces the voltage on the active switch to decease in resonant manner. After that, the active switch turns on with zero voltage switching.

The dead time delays are determine by the resonant switching durations due to the charging and discharging of C_r by the valley and peak inductor current (ΔI_L). To realize complete resonant switching transitions, there must be sufficient dead time at each of these transitions. If fixed dead time delay is used to achieve ZVS, its value

must be designed to cover the maximum required durations. They would always have to be longer than the ideal resonant transition durations; hence if the used dead time were shorter than the ideal resonant transition duration, the resonant wouldn't be completed. Then the resonate capacitor (C_r=C_{r1}+C_{r2}) can be calculated as [8]:

$$\Delta t_d \geq \frac{2C_r V_g}{i_{L\min}} \tag{1}$$

Figure 5 shows the gate source signal to SW_1 and SW_2 at full load. It also shows the drain-to-source voltage of the two switches and indicates that the problem of active switch is solved, but the body-diode of the synchronous switch turns on before the synchronous switch is turn-on, that creates body-diode loss. Note that as load changes, body diode loss changes also.

IV. ADAPTIVE GATE DRIVE TECHNIQUE

The adaptive delay control technique has very definite advantages over the fixed delay method. What if a feedback system were used to detect body-diode conduction, and actively adjust dead time delays to minimize it? Controlling the synchronous rectifier in this fashion would result in several key benefits, such as [9]:

- Could virtually eliminate body-diode conduction. Therefore, reverse recovery losses would also be significantly reduced.
- System would be adjusted for different MOSFETs, temperature and load dependent delays.

Figure 6 show the complete circuit of buck converter with voltage mode control by adaptive Gate Drive Technique. The operation of adaptive circuit depends on the voltage sensing at synchronous switch. When the voltage of synchronous switch is set to zero and PWM output also equals zero, the output of NOR gate is high which makes the synchronous switch on, but when the PWM is set to be high the synchronous switch turns off at this moment which make cross loop. Adaptive technique introduces a solution for body diode loss, but switching losses still there as it operate at hard switching PWM.

V. ZVS-QSW WITH ADAPTIVE TECHNIQUES.

Here ZVS-QSW and adaptive technique are merged together. Fig. 7 shows the complete circuit of ZVS-QSW with the application of adaptive technique. The advantage of this technique over the hard-switching adaptive technique is the saving of switching power loss by ZVS. As shown in Fig. 8, the transition from turn-on to turn-off occurs in soft switching and without body-diode conduction (adaptive). However, the same problem of adaptive technique at transition from OFF to ON is still occurring with cross-shooting, that requiring adding a fixed delay time backing into the same disadvantage for active switch. As a conclusion, merging adaptive technique with ZVS-QSW has a lot of advantages. However it needs more improvement for the turning on transition.

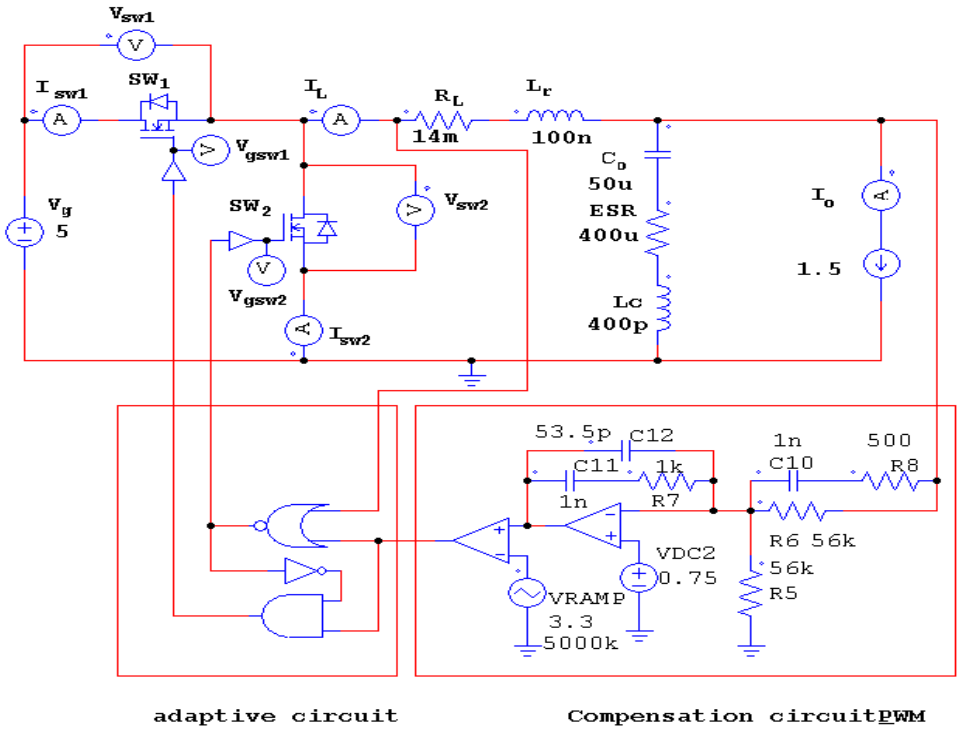


Fig.6 Complete circuit of adaptive gate control

VI. PROPOSED ADAPTIVE ZVS-QSW TECHNIQUE

The proposed technique is based on the natural analysis of the previous merging system to understand its problem and solving it. Fig. 8 shows the different stages of operation.

The initial *state* is [0-1], the two differential equations are:

$$L_r \frac{di_L}{dt} + v_{Cr} = V_o \qquad C_r \frac{dv_{Cr}}{dt} = i_L \tag{2}$$

Solving (2), the inductor current is obtained as:

$$i_L = i_{Lo}\cos(\omega t) + \frac{V_o - v_{Cr}(0)}{Z_o}\sin(\omega t) \tag{3}$$

The voltage on resonant capacitor on synchronous switch is obtained as:

$$v_{Cr}(t) = V_o + KSin\left(\omega t + \tan^{-1}\left(\frac{-(V_o - v_{Cr}(0))}{Z_o i_{Lo}}\right)\right) \tag{4}$$

$$where\ \omega = \sqrt{\frac{1}{L_r C_r}}\ \&\ Z_o = \sqrt{\frac{L_r}{C_r}} \qquad K = \sqrt{(v_o - v_{Cr}(0))^2 + (Z_o i_{Lo})^2} \tag{5}$$

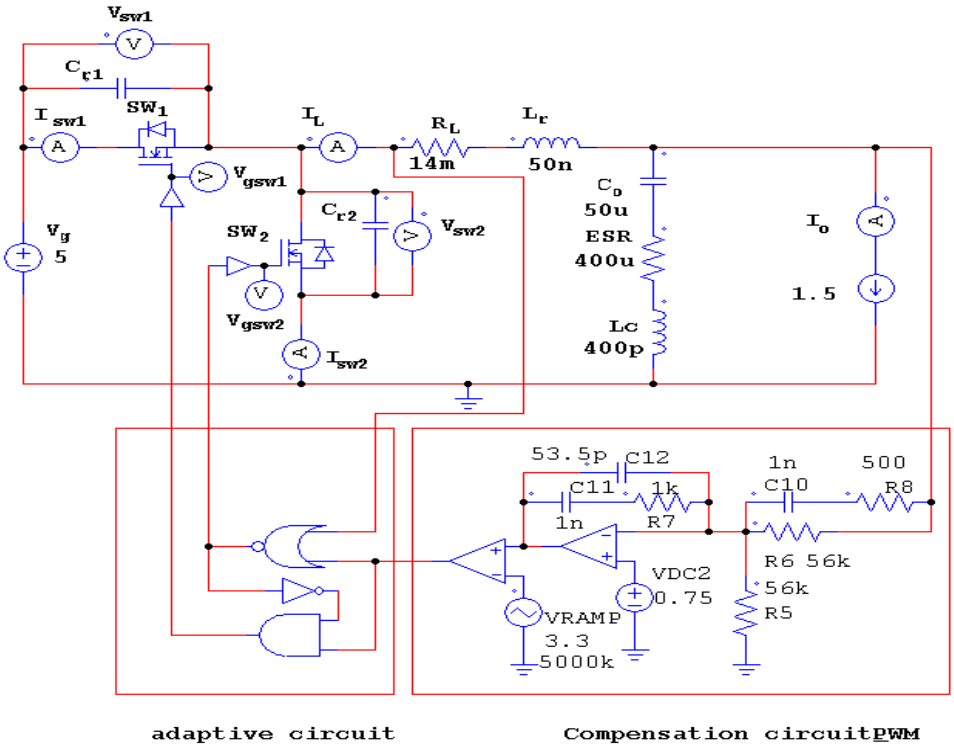
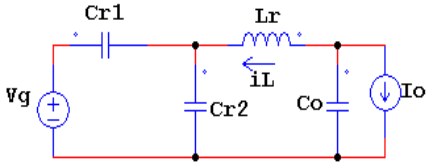
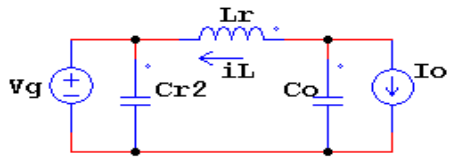


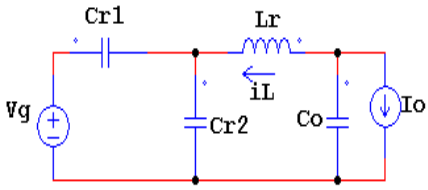
Fig. 7 ZVS-QSW using adaptive technique



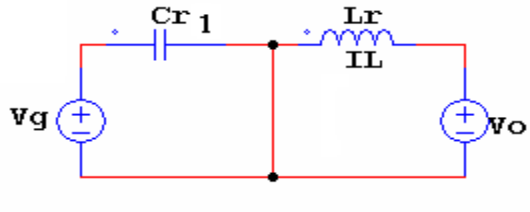
(a) Stage 1 [0-0]



(b) Stage 2 [1-0]



(c) Stage 3 [0-0]



(d) Stage 4 [0-1]

Fig. 8 ZVS-QSW adaptive gate drive technique stages

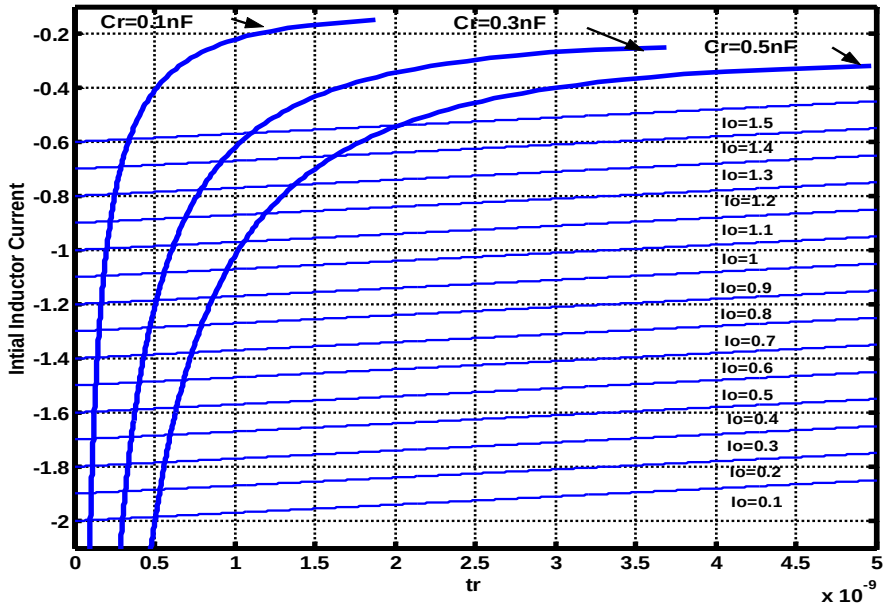


Fig. 9 Initial inductor current and required resonant time at different resonant capacitor values.

Stage 2 [1-0]: From Fig. 8(b), this is the ON stage.

Stage 3 [0-0]: From Fig. 8(c), the inductor current and output voltage are:

$$L_r \frac{di_L}{dt} + v_{Cr} = V_o \;\&\; C_r \frac{dv_{Cr}}{dt} = i_L \tag{6}$$

The inductor current can be derived as: $i_L = i_{Lo}\cos(\omega t) + \frac{V_o - v_{Cr}(0)}{Z_o}\sin(\omega t)$ (7)

The final equation of resonant capacitor voltage can derived as:

$$v_{Cr}(t) = V_o + K\,Sin\left(\omega t + tan^{-1}\left(\frac{-(V_o - v_{Cr}(0))}{Z_o i_{Lo}}\right)\right) \tag{8}$$

Where $K = \sqrt{(V_o - v_{Cr}(0))^2 + (Z_o i_{Lo})^2}$ (9)

Stage 4 [0-1]: This is the regular OFF stage.

The proposed technique is based on the analysis for ZVS-QSW adaptive technique. From previous analysis, after the active switch turns off, both of switches are off (Stage 3) and the initial capacitor voltage $v_{cr2}=V_g$. The required soft switching technique order is to force the capacitor voltage to damp into zero, then turning on the synchronous switch. Applying this into Eq.(8) and putting the final value equals zero, the required time to achieve ZVS is:

$$t_f = \frac{sin^{-1}\left(\frac{-V_o}{K_1}\right) - tan^{-1}(\theta_1)}{\omega}$$

Where $\theta_1 = \left(\frac{-(V_o - V_g)}{Z_o i_{Lo}}\right)$, $K_1 = \sqrt{(V_o - V_g)^2 + (Z_o i_{Lo})^2}$ (10)

Finally, before the active switch is turn-on, the synchronous switch is off. So the initial capacitor voltage $v_{Cr2} = 0$ and its required final value is V_g. Applying this into Eq.(4), then the required time to raise the capacitor voltage into V_g is:

$$t_r = \frac{\sin^{-1}\left(\frac{V_g - V_o}{K_2}\right) - \tan^{-1}(\theta_2)}{\omega}$$

Where $\theta_2 = \left(\frac{-V_o}{Z_o i_{Lo}}\right)$, $K_2 = \sqrt{(V_o)^2 + (Z_o i_{Lo})^2}$ (11)

Recalling the previous problem of ZVS-QSW with adaptive technique that cross-shooting occurs at on transition. There, a dead time equal to t_r to achieve ZVS. The t_f time is already applied by adaptive technique at different resonant capacitors. From Eq (11), the time required to make the capacitance voltage reaches the input voltage (active switch voltage reaches zero) depends on the initial value of inductor current i_{Lo}. The required time t_r at each initial current i_{Lo} for each capacitor value is shown in Fig. 9. Also, the required initial current for each load current is drawn in the same figure. The intersection points give the required dead time to bring the resonant capacitor voltage into the input voltage achieving ZVS operation for the active switch. From this figure, it is cleared that as the summation of resonant capacitor C_r increases, the required dead time t_r increases. Moreover, moving towards light load required a smaller dead time with higher initial inductor current to prevent the conduction of body-diode of active switch. Fig. 10 gives the relation of the required initial inductor current for each load current at each resonant capacitor. From Fig. 10, the required initial current and its equivalent rise time t_r at each resonant capacitor value can be obtained. Then, acceptable values of capacitance have been chosen, 0.1µF, 0.3µF and 0.5µF.

The problem of previous topology of ZVS-QSW adaptive technique is the crosses shooting between active switch and synchronous switch at on transient. This problem can be solved by making the synchronous switch turn off before active switch turn on by dead time sufficient to perform ZVS (turn on at zero voltage). By using Fig. 10, the initial current required at 1.5A is -0.54A at C_r =0.5 nF, so the synchronous switch must be turned off at i_L= - 0.54A, for example. Therefore adjusting the system to turn off and inductor current reaches this predetermined value at every load current can achieve the soft switching of the turn-on transition. Based on this novel technique a proposed circuit is presented here. Fig. 11 shows the complete circuit of the presented topology. A new current sensor is added to sense the inductor current and compare it with the predetermined value at the initial current. As this value matches, the

comparator generates a signal to turn off the synchronous switch. During this off (stage 1), the drain voltage reach the input voltage.

Figure 12 (a) shows the gate signals and drain- source voltages of both switches. It is cleared how the perfect operation is achieved. Both turn-on and turn-off transition is done on ZVS techniques. There is no body-diode loss. More details can be obtained from Fig. 12 (b). SW 1 turns on and off at zero voltage. So the switching losses are eliminated. Also, Fig.12 (c) shows the waveforms of the current and voltage of SW 2. Also, it is clear that the switch turn on and turn off occur at zero voltage.

Moreover, the operation of presented topology at 0.5A (30% load) is shown in Fig.13 to show the operation at light load and prove the advantage of the proposed technique. As a conclusion, this technique has solved all previous listed problems.

To conclude all studied topologies and techniques, a comparison of efficiency at different loads demonstrated by using PSIM. The tested circuit is 5MHz Synchronous buck converter with 5V input and 1.2V/1.5A output. All detailed circuit parameters will be included in the final version due to space limitation here.

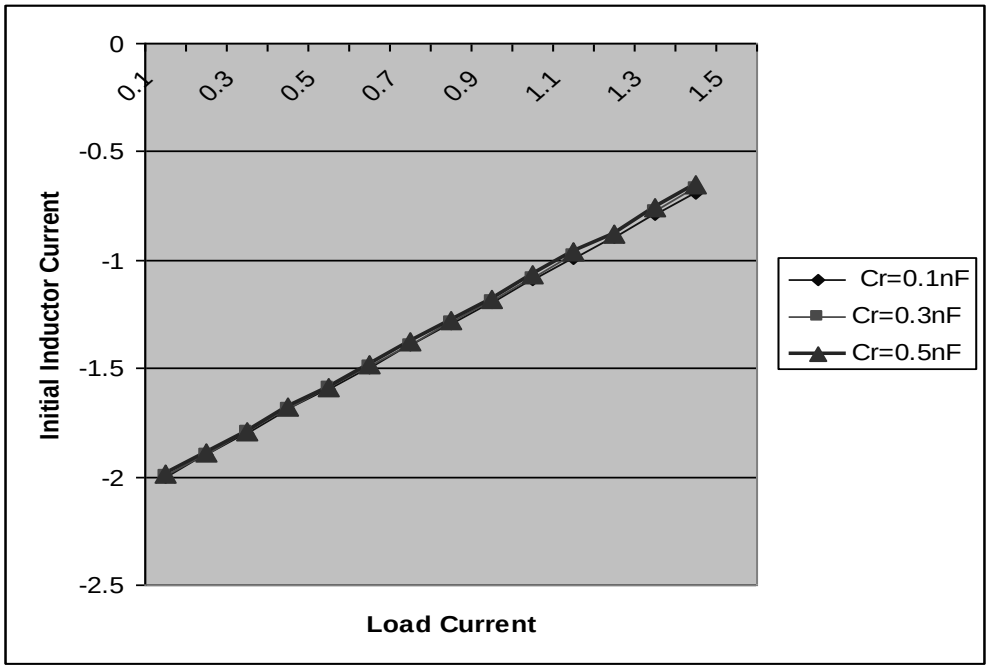


Fig.10 Initial inductor current at different loads and different capacitors.

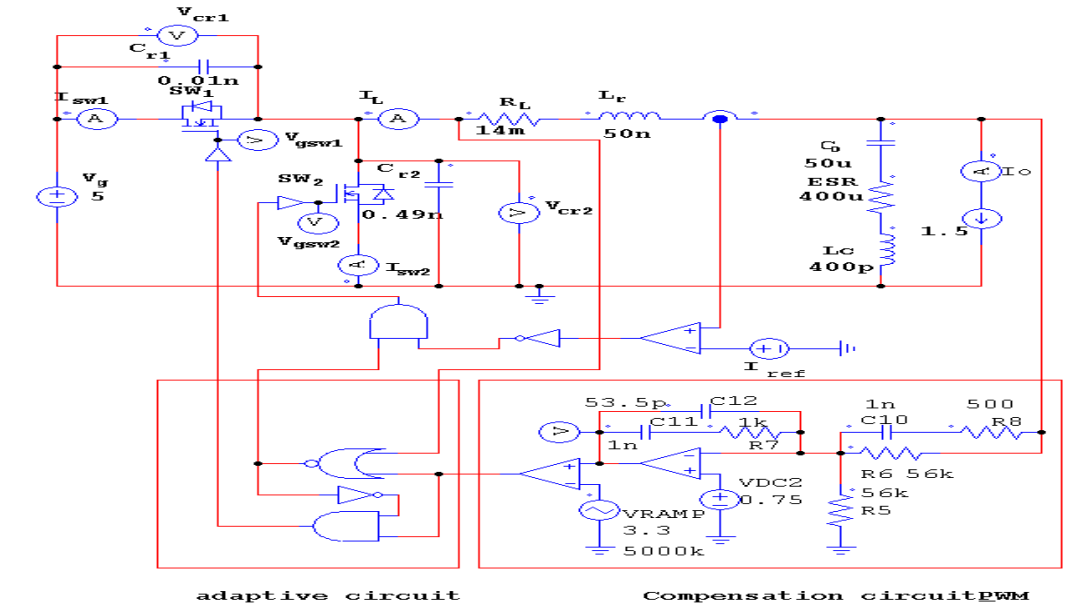
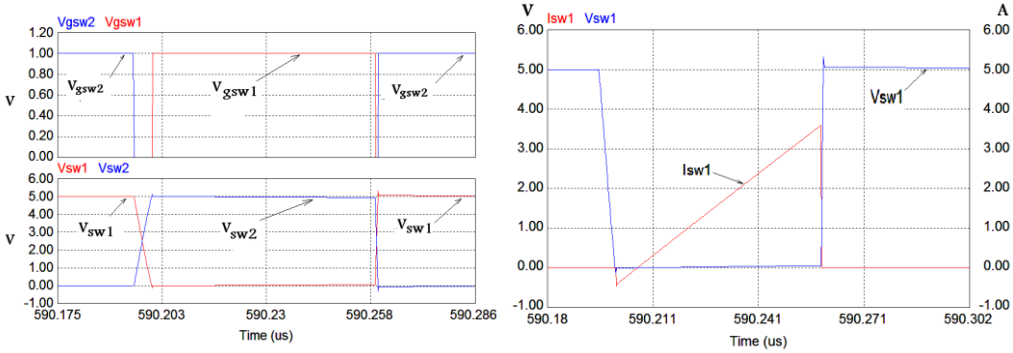
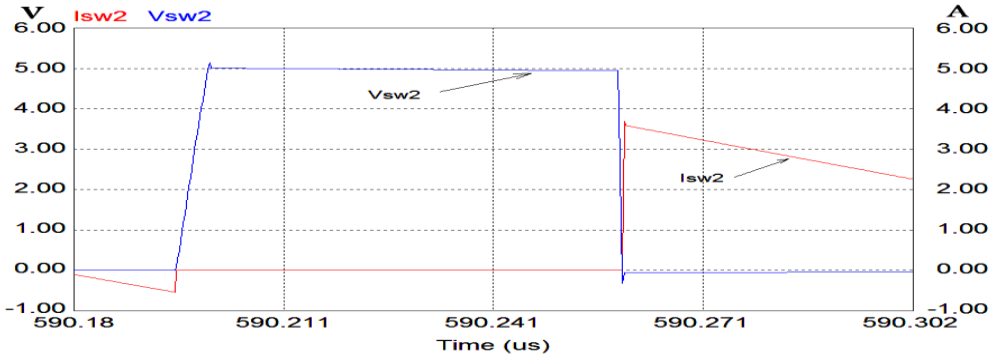


Fig. 11 Complete circuit of proposed technique.

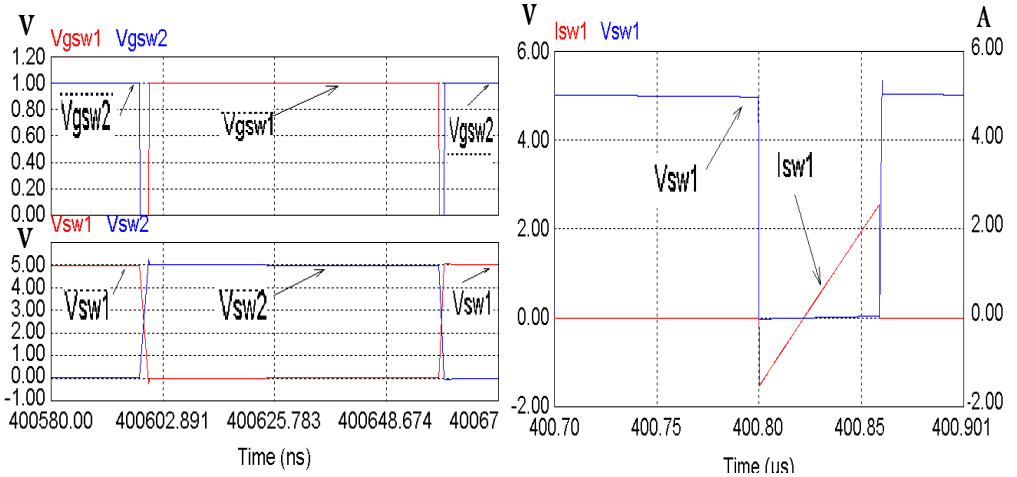


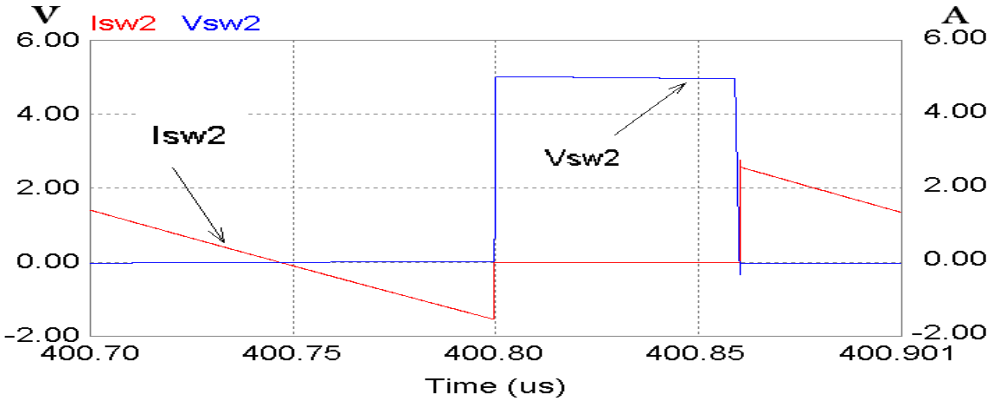


(a) Gate signals and drain source voltages (b) Voltage and current of switch 1.
(c) Voltage and current of switch 2.

Fig. 12 The proposed adaptive ZVS-QSW technique operation at full load.

Figure 14 shows the overall efficiency of PWM, ZV-QSW fixed dead time, hard switching using adaptive, combined ZVS-adaptive and new proposed preprogrammed adaptive ZVS-QSW technique. It's clear that the proposed technique achieves the highest efficiency over all load currents. About 6% has been increased in efficiency at full load which means saving in switching and body-diode losses. Another at light loads, a great improvement in the efficiency is obtained (about 35 points improvement over the hard switching and 15 points over the previous adaptive technique). Therefore, the new proposed technique is achieving the best operation with saving the switching and body-diode losses results in high efficiency values over the load range that is required today for most applications. As declared above, the theoretical analysis has been proven by simulation.





(a) Gate signals and drain source voltages (b) Voltage and current of switch 1.
(c) Voltage and current of switch 2.

Fig. 13 The proposed adaptive ZVS-QSW technique operation at 30% load.

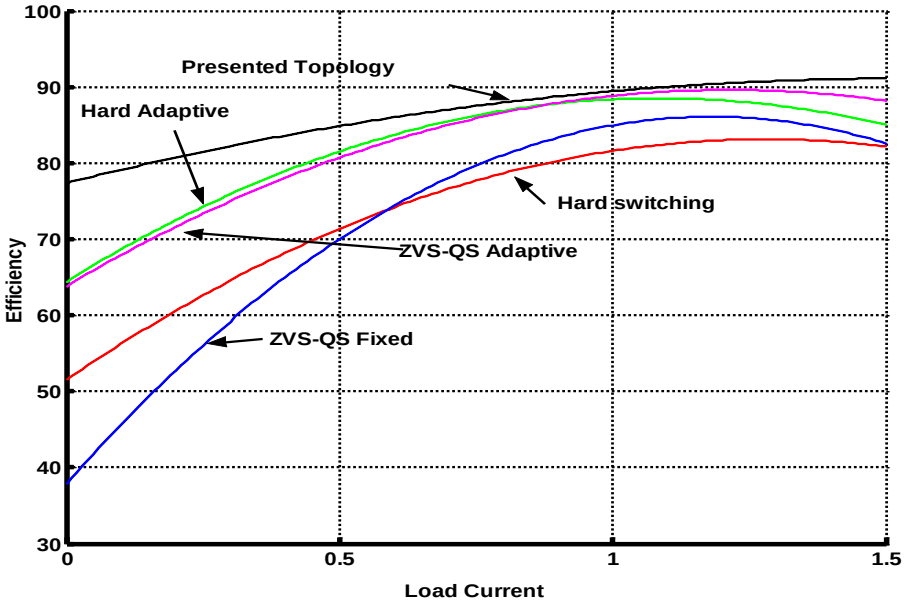


Fig. 14 The overall efficiency of all different techniques.

VII. CONCLUSION

Two new techniques have been proposed. First technique has been proposed by merging ZVS-QSW with adaptive technique to take the advantage of both. This technique has the limitation to solve for active switch turn-on transion. Therefore, the second proposed technique adds a programmed comparator for the inductor current to force achieving the ZVS for the turn-on transion of the active switch. Using this technique higher efficiency values have achieved over the load range. More than 6% improvement at full load and 15% improvement under light load have been achieved. Simulation results have confirmed the proposed theory. Moreover, the advantage of applying quasi square technique is using a very small value of the output filter as low size inductor L_o is used. It's very important advantage that works in the same direction of integrated circuit.

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تقنية جديدة للفصل الناعم للمغير الخافض التزامنى معتمدة على دمج تقنية الفصل عند جهد يساوى صفر بموجة شبة مربعة مع تقنية التكيف

فى الوقت الراهن الهدف الاساسى أمام مصممى مغذيات القدرة هو تغذية الاجيال الحديثة من المعالجات الميكروئية ومعالجات الاشارات الرقمية لذلك فهى تحتاج إلى معدل كبير فى تغير التيار يتوافق مع جهد الخرج الصغير والشيئ المهم فى تلك المغذيات هو الكفاءة وخصوصا مع التردد الفائق حيث أن استخدام التردد العالى له مساوئ من أبرزها مفاقيد الفتح والغلق للمفاتيح وأيضا مفاقيد التوصيل للثنائى الموجود فى المفاتيح.

لذلك فإن تقنية تشغيل المفاتيح عند جهد يساوى صفر مع استخدام موجة شبة مربعة قد درست لكى تقدم حلا لمفاقيد الفتح والغلق ولكن هذا الحل لا يمكن ان يطبق لمدى تيار كبير. وتقنية التكيف استخدمت لتتقليل مفاقيد الثنائى. لذلك فإن هذا البحث قدم حلا بدمج الطريقتين معا للاستفادة من مميزتهما معا. بالاضافة الى ان البحث قدم دائرة جديدة طبقت على تقنية الفصل الناعم للمفتاح الاساسى. وفى الخلاصة فإن البحث قدم طريقة جديدة فى الفصل الناعم عند التردد العالى للمغير الخافض التزامنى معتمدة على تقنية الفصل عند جهد يساوى صفر بموجة شبة مربعة مع تقنية التكيف. وتناول البحث المعادلات الرياضى ونتائج برنامج المحاكاة عند تردد 5 ميجا هرتز.