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Design of integrated all Optical JK flip flop using 2-D photonic crystals

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Keywords
Photonics crystal, optical JK flip flop, logic gates, resonance cavity PCRR, Optical memory, optical CPU

Abstract: A novel all optical JK Flip Flop design is presented based on 2cDimension photonic crystals (PhC). The overall size of the designed JK flip flop is 80 μm × 40 μm of 2cDimension square lattice photonic crystals with a refractive index equal to 3.4 placed in air. The band gab is equal (a/λ) = 0.321 to (a/λ) = 0.441 corresponding to the wavelength range 1550 nm< λ <1560 nm. The lattice constant 'a' of the structure is equal to 630 nm. The design of optical JK flip flop is based on the nonlinear 3x3 and 9x9 photonic crystal ring resonator. The proposed J-K flip flop has been designed, analysed, and time dependent simulation results are standing on the finite difference time domain (FDTDc) and Plane Wave Expansion (PWEc) methods to confirm its operation and feasibility.

1. Introduction

All optical logic devices based on the Photonic crystals (PhC) are considered as main devices to handle a large bandwidth signal at very high speed in present all optical signal processing systems and the future optical networks [1, 2]. Consequently, it is necessary to move towards all optical processing units, to overcome the electronic bottlenecks speed and fully exploit the advantages of optical fibre communication system and photonics crystals, where the data will remain in the optical without optical to electrical conversion and vice versa [1-3]. The optical flip flop can be used to perform a fast central Processing unit (CPU) and optical memory using optical hardware components [4-6] such as the photonics crystals. In addition, the specs of the photonic crystals structures make them very promising for designing ultra-compact size optical devices in the integrated circuits [7- 9].

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The novel proposed optical integrated JK flip flop is introduced using a 2-D photonic crystal to use the speed and increase the performance of the optical network, optical memory, and optical CPU [1]. In recent years, many papers have proposed optical digital devices such as logic gates, digital comparator, Decoders, Encoder, Multiplexer, DE multiplexer, half adder, and full adder by using the photonic crystals [10-26], moreover many all optical SR and D flip flops have been proposed [27, 28, 29].

None of all previous PhC's and optical logic design performs any JK flip flop by using the integrated 2D photonic crystals which is important for optical digital processing. Therefore, this paper presents a novel design of JK optical flip flop by using 2-D square lattice photonic crystals. The designed JK flip flop is the extension of our designed SR flip flop presented in Tamer et al. [27], where the design is modulated by two 9x9 photonics crystal ring resonators (PCRR's) to perform and realize the operation of J-K flip flop. The J-K flip flop is considered the major device in the design of sequential logic circuit [30-33], so that the optical JK flip flop may be help in the design of All optical counters [27, 34]. The 2-D photonic crystals are widely used according to fabrication in integrated circuits.

2. 9 X 9 PCRR.

Figure 1 shows the structure of the PCRR which was fabricated by eliminating a matrix of 9x9 arrays of dielectric rods to create a resonance cat wavelength of 1550 nm [18, 35] in which, the rod radius is equal to $r = 0.2\,a$, where s is the distance between two neighbour rods.

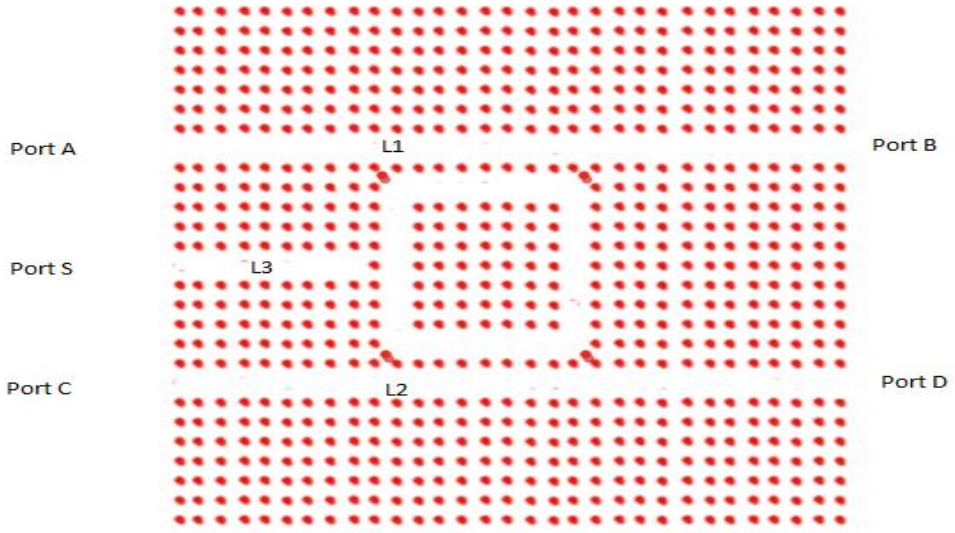
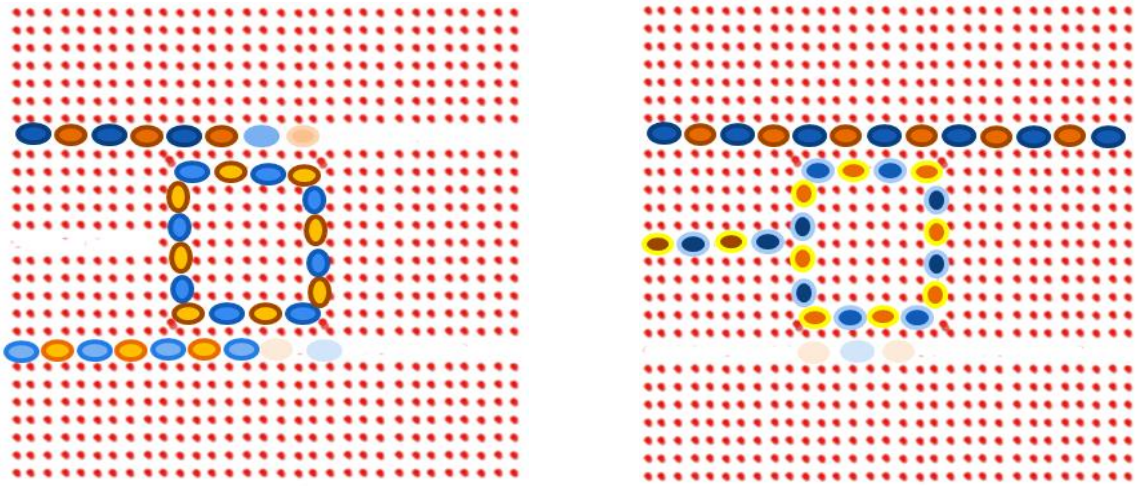


Fig.1. The schematic structure of 9x9 PCRR [33]

An optical signal of wavelength λ=1550 nm is used to excite the PCRR from input bias port (A), and the output is obtained from one of output ports (B, C, D) according to the controlled signal lunched from the port (S) [18]. At S=0, The bias optical signal of port A is coupled into

the ring and flows to the port (C) as shown in figure 2 (a). At S=1, the output obtained from port (B) which enhances the field intensity in the ring and prevents the coupling of the port A input with the ring resonator as shown in figure 2 (b) [18, 35]. According to the previous operation, this PCRR can be used as optical AND logic gate between S, A as inputs, and the port B as output of the gate.



(a) (b)

Fig. 2. The Field pattern of 9x9 PCRR at (a) S=0, and (b) S=1. [35]

3. J-K Optical Flip Flop in the integrated 2-D photonic crystals.

Figure 3 shows the circuit diagram of digital logic J-K flip flop [30], where the J-K flip flop is considered a universal flip-flop circuit [31]. The J-K flip-flop has four possible inputs combinations, “no change”, “logic 0”, “logic 1”, and “toggle” as shown in logic truth table 1.

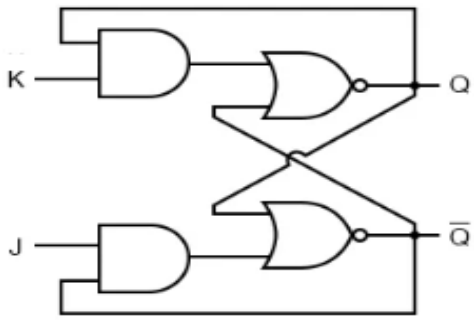


Fig.3. J-K flip flop logic circuit diagram [30].

Table 1. J-K flip flop truth table

J	K	Q_{n+1}	Q'_{n+1}	State
0	0	Q_n	Q'_n	No Change
0	1	0	1	Reset
1	0	1	0	Set
1	1	Q'_n	Q_n	Complement

Figure 4 shows the structure all optical J-K flip flop of 80 μm ×40 μm 2-D PhC. The lattice constant 'a' is equal to 630 nm with a rod radius equal to 0.2ac, which is closed to 126 nm. The design is based on the photonic crystal S-R flip flop that published before [27]. In addition to, two additional 9x9 PCRR are used as two AND gates. The first AND logic gate is constructed byc9x9 PCRR5 which cross coupling connection between input J and Q'. Consequently, the second AND logic gate is constructed by another 9x9 photonic crystal ring resonator PCRR6 which cross coupling connection between input K and Q.

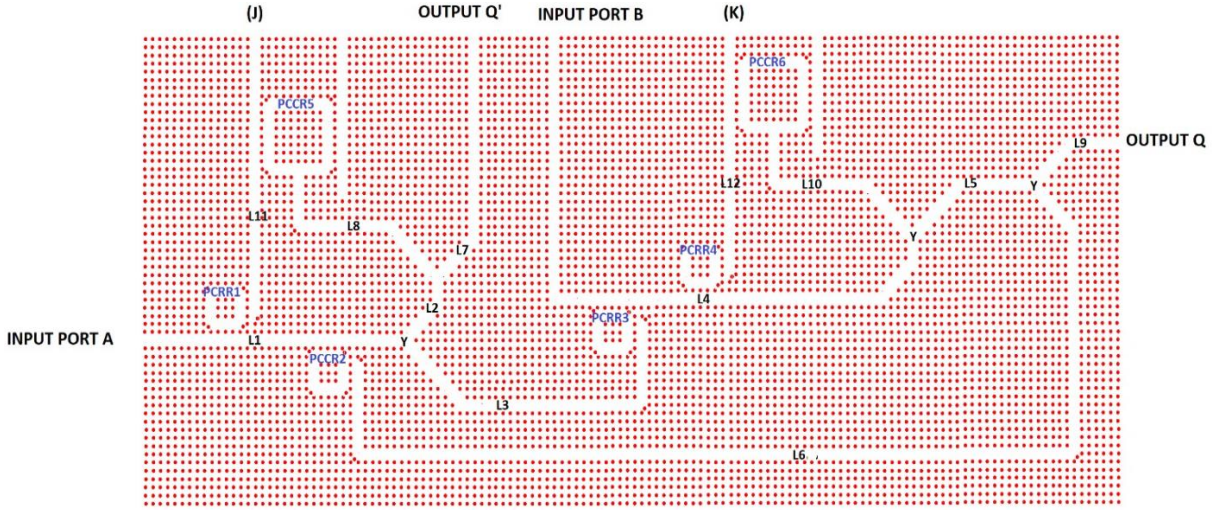


Fig. 4 All-optical J-K flip flop in 2D Photonic Crystal

PhC- J-K flip flop consists of four 3x3 PCRR (PCRR 1 to PCRR 4) with radius of 3a with a set of Y splitters and T-type waveguides (L1 to L12). Where, these 3x3 PCRR's are used to construct the optical NOR gates of the flip flop. The outputs of each NOR gates are splitting by two square lattice Y splitter with transmission efficiency of 47 % and splitting ratio of 50:50 [27, 36]. The waveguides optical signals of L1 and L4 are splitting into two waveguides (L2, L3) and (L5, L10) respectively with optical power of 48 % from the optical power in the main waveguides optical signal of L1 and L4. Also, the waveguides optical signal of L2 and L5 are splitted into two waveguides (L7, L8) and (L9, L6) respectively with optical power of 48 % from the optical power in the main waveguides optical signal of L2 and L5.

The ports A and B are used to excite the optical J-K flip flop optical signal and exit from ports Q and Q\. The inputs-K of flip-flop are applied to one port of AND gates and other input is obtained from feedback of outputs Q and Q\ as a trigger input for 9x9 PCRR by using the optical y splitters. Consequently, the outputs of each AND gates are directed to control a certain port for each NOR, and the other control signal ports for each NOR gate are obtained from feedback of outputs QC and Q\ respectively through the optical y splitters. The Ports B and J has optical wavelength equal to λ1=1550c nm, while the wavelength of port Acland K are equal to λ2=1560c nm, where A and B ports are biased by light intensity of 200 mw.

Extractors are shifted toward the corner of 0.707a with the same refractive index are placed at the corners of all PCRR's and waveguides to eliminate the back scattering at operating wavelengths of ports J and K, which is derived by the plane wave expansion (PWEc) method. Figure 5 shows the band gab range of the photonic crystals along the most symmetrical lines (ΓX, XMc, MΓc) for the overall structure which is derived by the plane wave expansion (PWE) [37] and the finite difference time domain FDTDc [38] methods. The band gab range is equal ca/λ= 0.321 to ca/λ= 0.441 according to the wavelength range 1550 nmc< λ <1560 nmc. The photonic crystal designed with a band gab range of a/λc keeps the light travel and prevents photons in the band gap from propagating in the material that is propagating only in the waveguide [34].

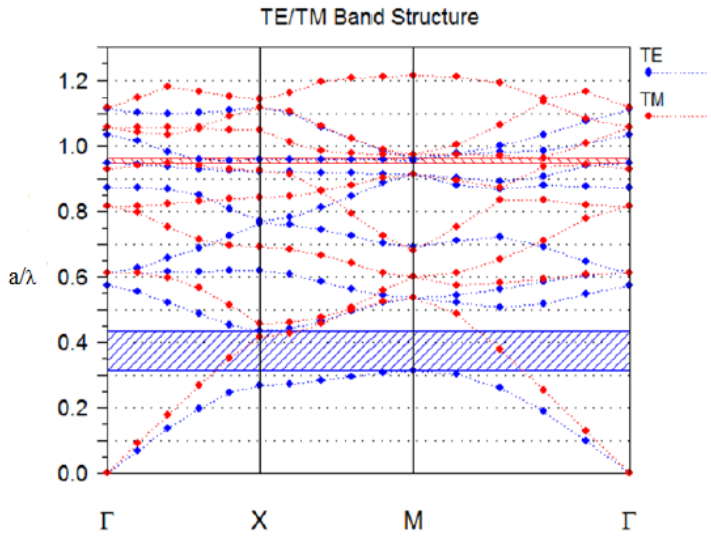


Fig.5. The diagram of band gab structure at r=126 nm.

4. The structure realization and the simulation results of optical J-K flip flop.

The results and performance of the proposed optical J-K flip flop are depicted in this section. As presented before, the proposed novel optical JK flip flop is based on the principal operation of SR flip flop in [27] with modifications that have been added to the overall system to construct two optical AND gates. Here, we consider sequence of input lights (J-K) with initial state for Q=0c and Q'=1c at time t1 as shown in figure 6 (a) to realize the operation of proposed J-K flip-flop. The operations are as follow:

Case 1c (Toggle -Complement Q): - Suppose that in time t2, the present state of Q=0 and Q'=1 at J=K=1 as depicted in figure 6 (b). The digital logic output Q'= 1c (44cmw) prevents the coupling of the optical binary signal (J) into PCRR5 and forwards it through the waveguidecL11 towards PCRR1. This coupling prevents the optical signal of port A from passing and change the output Q' to logic 0. In addition to the optical signal of logic input K=1 is dropped to PCRR6 as depicted in figure 6 (b). So that, at steady state of No change case with J=K=0 [27] in time t3, the optical signal of port B is passing through two Y splitters

and reaching to output Q=1c(44cmw), and feedback again to PCRR2 as a second input to other NORcgate2 as shown in figure 6 (c) to keep the output Q'=0.

Case 2 (Toggle -Complement Q'): - At time t4, J and K are switched to logic 1 again at present state of Q=1 and Q'=0 as shown in figure 6 (d). The output Q= 1c (44cmw) prevents the coupling of the optical signal (K) into PCRR6 and forwards it through the waveguide L12 towards PCRR4, where optical signal in PCRR4 with the optical signal of port B changes the output Q to logic 0. In addition, the optical signal of logic input J=1 is dropped to PCRR5 as shown in figure 6 (d). So that, at steady state of No change case with J=K=0 in time t5, through the Y splitters and waveguides the optical signal of port A maintain the output Q' at 1 (44 mw), and feedback again to PCRR3 as a second input to other NOR gate2 such as figure 6 (a) to keep the output Q=0.

Case 3 (Set Case): - At time t6, suppose that J is switched to 1 and K is still equal to 0 as shown in figure 6 (e) at state of Q=1 and Q'=0. The digital logic output Q= 1 attenuates the coupling of the optical binary signal (K) into PCRR5 and forwards it through the waveguidecL11 towards PCRR1 which attenuates the optical signal of port A and changes the output Q' to logic 0. So that, at steady state of No change case with J=K=0 in time t7, the optical signal of port B is propagating and output Q becomes equal to 1 (Q=1), and feedback to PCRR2 such as figure 6 (c) to keep the output Q'=0.

Case 4 (Reset Case): - suppose that in time t8, K is switched to 1 and J is still equal to 0 as shown in figure 6 (f) at present state of Q=1 and Q'=0. The digital logic output Q= 1 prevents the coupling of the optical binary signal (K) into PCRR6 and forwards it through the waveguide L12 towards PCRR4 which attenuates the optical signal of port B and changes the output Q to logic 0. So that, at steady state of No change case with J=K=0 in time t9, the optical signal of port A is propagating and output Q' becomes equal to 1 (Q'=1), and feedback to PCRR4 as shown in figure 6(a) to keep the output Q=0.

Figure 7 shows the mechanism of the optical JK flip flop with all previous different states. The experimental normalized output results backed by FDTDc and PWEc methods is depicted in Figure 8. All waveforms depicted in figure 8 are scaled arbitrary. The transient switching of flip flop takes rise time of output tr= 3.95 ps, steady state time tss=6.26 ps, and fall time tf=1.18 ps as depicted in table 2, which compared these parameters with the parameters of SR flip flop presented in Tamer et al. [27]. The speed of this J-K flip flop can be reaching cup to 200 GHz, which helps to obtain high-speed central processing unit and eliminates the speed limitation in optical networks, and optical signal processing. The proposed optical JK flip flop has a high insertion loss for these states of inputs. Moreover, the results of the proposed design show considerable performance for optical signal processing. Consequently, the designed optical JK flip flop can be easily fabricated, where the photonic crystals integrated circuit reduces the size of optical components to sub nanometres. These mentioned advantages make the proposed JK flip lop to be used in the design of all optical N bit Asynchronous counter, Synchronous counters, and sequential logic circuits [34].

Table 2. Comparison between SR flip flop [27] and the proposed JK flip flop.

Items	J K Flip Flop	S R flip flop
Size	80 μm × 40 μm	30 μm × 30 μm
Rise time	3.95 ps	3.89 ps
Fall time	1.18 ps	1.18 ps
Steady state time	6.26 ps	6.25 ps

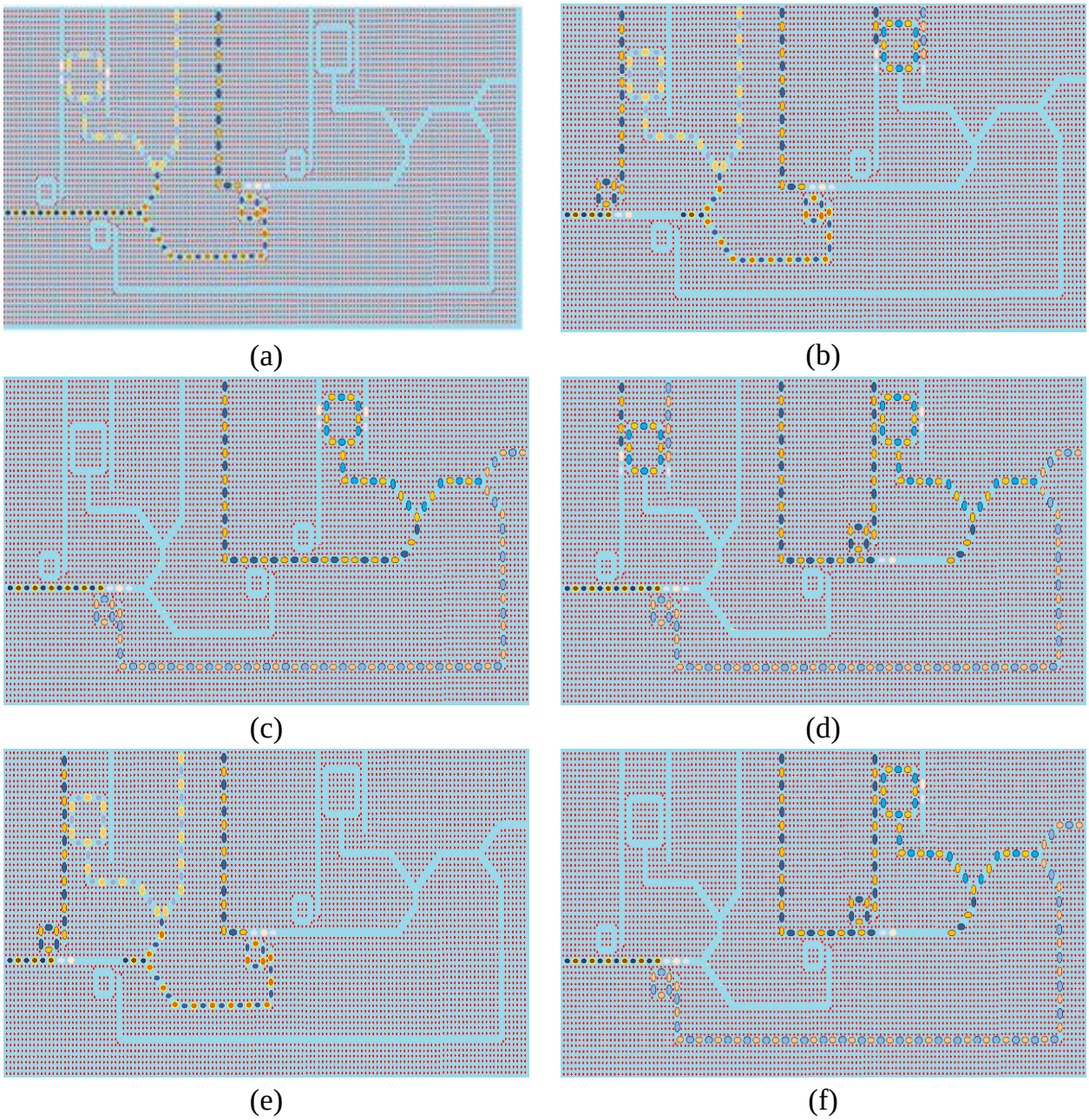


Figure 6 Steady state electric field patterns of all optical J-K at (a) Initial state of Q=0 , and Q'=1 at J=K=0 , (b) Toggle state at J=K=1 with present state of Q=0 , and Q'=1 (C) J=K=0 (No change) with Q=1 , and Q'=0 , (d) Toggle state at J=K=1 at present state of Q=1, and Q'=0, (e) Set State at J=1, and K=0, (f) Reset state at J=0, and K=1.

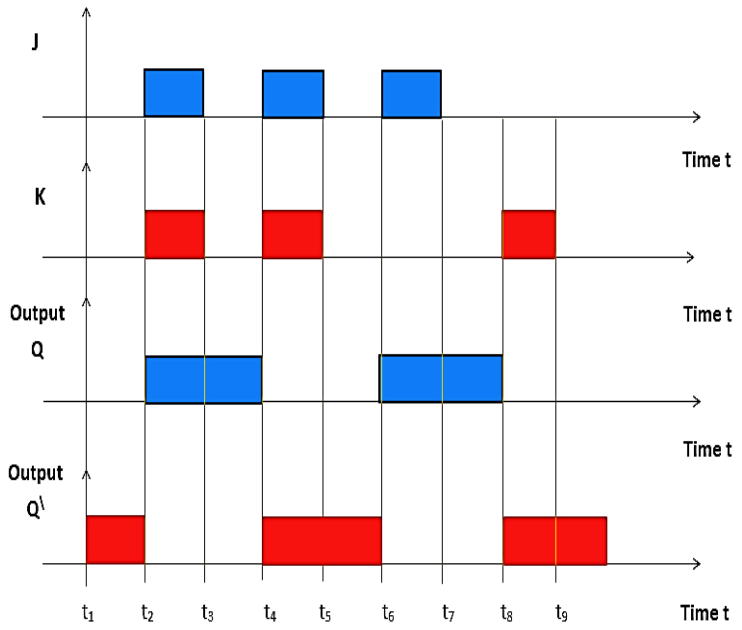


Fig.7. The time graph of the different states of JK flip flop.

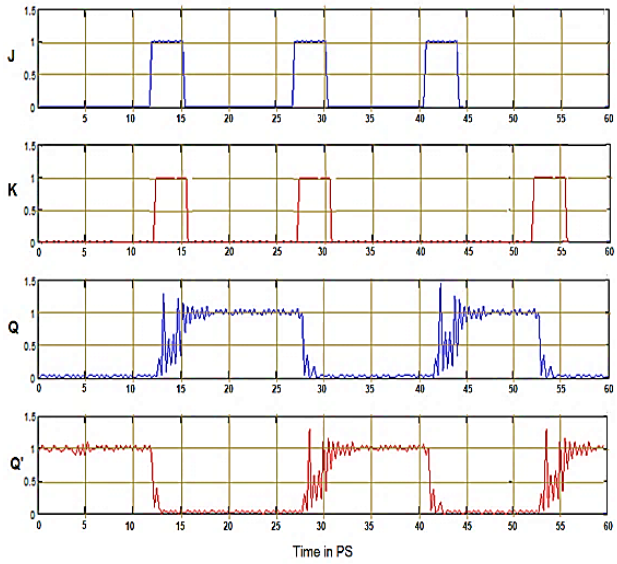


Fig.8. The time response simulation results of the all-optical J-K flip flop at duration width of 3 ps.

7. Conclusions

The paper proposed an all optical JK flip flop by using the photonic crystal's structure based on optical SR flip. The design of optical JK flip flop is based on the nonlinear 3x3 and 9x9 photonic crystal ring resonator (PCRRc), L waveguides, and Y splitters to connect between the PCRR's. The optical JK flip flop can be used to solve the bottleneck problem speed limitation for optical digital processing systems and optical networks. The structure is simulated by the finite difference time domain (FDTDc) and Plane Wave Expansion (PWEc) methods to confirm its operation and feasibility.

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تصميم هزاز بصري من النوع jk باستخدام البلورات الضوئية المتكاملة ثنائية الأبعاد

الملخص:

هذا البحث يقدم تصميما لهزازت بصرية من النوع J-K بأستخدام البلورات الضوئية ثنائية الأبعاد. الحجم الإجمالي للهزاز من النوع J-K المصمم هو ٨٠ ميكرومتر × ٤٠ ميكرومتر من البلورات الفوتونية على شكل شبكي مربعة الأبعاد ذات أبعاد ثنائية مع معامل انكسار يساوي ٣,٤ موضوعة في الهواء. مدى فجوة النطاق المستخدمة(λ/a) = ٠,٣٢١ إلى (λ/a) = ٠,٤٤١ و ذلك طبقا لطول الموجي مداه ١٥٥٠ نانومتر< λ <١٥٦٠ نانومتر. ثابت الشبكة "a" للهيكل يساوي ٦٣٠ نانومتر. و يعتمد تصميم الهزاز JK البصري على الرنان الحلقي البلوري الضوئي غير الخطي 3x3و9x9 . و لقد تم تصميم وتحليل تقنية الهزاز J-Kالمقترحة وتم وضع نتائج المحاكاة المعتمدة على الزمن على طرق فرق الزمن المحدود (FDTD) وطرق توسيع الموجة المستوية (PWE) لتأكيد جدوى التشغيل .