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An Efficient Fully Bootstrapped RF-to-DC Rectifier for Implantable Biomedical Applications in CMOS Technology

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Biomedical implants, bootstrapped rectifier, power conversion efficiency (PCE), wireless power transfer (WPT)

Abstract: This paper introduces a high-efficiency and a wide-frequency band RF-to-DC rectifier with an enhanced voltage conversion ratio (VCR) for implantable biomedical devices. The rectifier utilizes bootstrapped CMOS devices for threshold potential reduction. These devices (NMOS and PMOS) have bootstrapped gates. This is used to reduce the needed RF input voltage which turns rectifying devices ON, effectively adding DC voltages (positive or negative, respectively) to the input RF signal. This allows rectifier devices to conduct at lower input RF voltage levels. The proposed RF-to-DC rectifier circuit is designed and simulated in 180nm CMOS technology. Simulation results show a peak power conversion efficiency (PCE) of 81.3% at RF input power of -12.4dBm, with a load resistor and capacitor of 12 kΩ and 1pF, respectively. With the same loading, the proposed rectifier achieves a peak VCR of 87% at RF peak voltage of 1V. The obtained dynamic range of the proposed circuit is 15.7dB (PCE > 30%) at an input frequency of 402MHz. With an input frequency of 434MHz, the proposed circuit has a PCE of 80.85% at -12.8dBm RF input power, while having a load resistor and capacitor of 12 kΩ and 1pF, respectively. The rectifier achieves 87.14% VCR, and a dynamic range of 15.4dB (PCE>30%).

1. Introduction

In recent years, cardiovascular and neurological diseases have spread and are seen hard to treat with traditional medicines alone. This pushed researchers turning to research and development in the use of implantable medical devices which would greatly help in treating such diseases [1]. However, there were many challenges in real-life applications due to implantable devices charging difficulty. But, there was a window for devices powering

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wirelessly. This might diminish the need for repeated surgeries for battery replacement or device charging, so wireless power transfer (WPT) was suggested [2]. With wireless power transfer (WPT), devices can be powered and charged without the need for wires or unsightly connections, making them more user-friendly. Additionally, by advances made in batteries lifetime and capacities, implantable biomedical devices lifetime can be extended.

As smaller devices are favoured and cables can become inconvenient and unreliable over time owing to wear and tear, WPT has grown increasingly in recent years and has become a focus in both research and commercial product development. WPT, as opposed to cable-based solutions, guarantees excellent longevity and dependability, especially in harsh situations like those seen in biomedical monitoring and treatments, and underwater applications [3], [4].

Depending on how energy is transmitted, far-field WPT (radiative technique) - in which the energy is transferred by microwave power transfer [5] - or near-field WPT (nonradiative method) -in which the energy is transmitted utilizing magnetic or electric fields can be employed [6], [7], [8], [9] . Fig. 1 shows a system block diagram of wireless power transfer (WPT). As shown in Fig. 1, to realize the interface between transmitter (TX) and receiver (RX), the coupling block which receives power from the TX and couple it to the RX should be carefully designed. Usually, driver and power stage make up the TX. Rectifier and voltage regulator are forming the RX side. If a bidirectional communication channel is required, TX and RX are modified to adjust the transmitted power upon RX requirements and TX capabilities employing some additional control circuits [4].

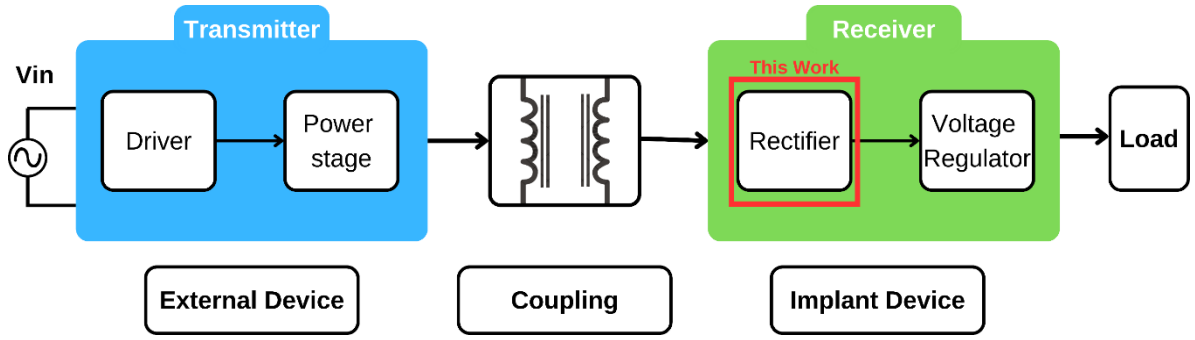

Fig. 1: Wireless power transfer block diagram.

One of the practical applications of the WPT system is upper limb rehabilitation. Used for individuals recovering from conditions like stroke or spinal cord injuries with the help of electrical muscle stimulation (EMS)[10], [11] as shown in Fig. 2. Fig. 3 shows the block diagram of the implantable RF energy harvesting system. This starts with the receiving antenna, which captures the power from the external transmitter. The implantable antenna is designed to be suitable and safe for the human body. The antenna design challenges contain small size, high power efficiency, and it should be made of biocompatible material. In [12], [13], [14] implantable antennas for ISM frequency bands (such as 402MHz, 434MHz). The ISM frequency band. ISM refers to (Industrial, Scientific, and Medical), this band can be used without specific permission.

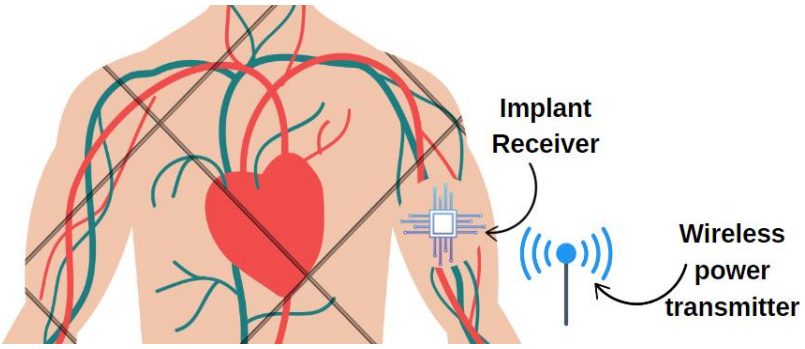

Fig. 2: Upper limb stimulation.

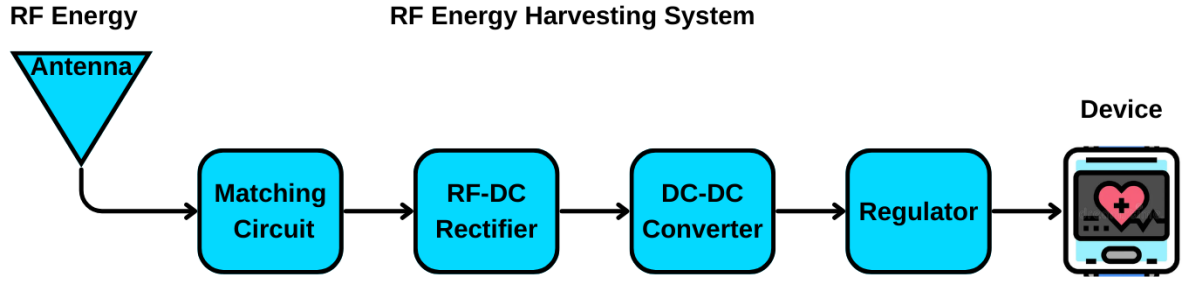

Fig. 3: RF Energy Harvesting Receiver

Impedance matching, the second circuit, maximizes power flow from the antenna to the rectifier while minimizing reflection losses[15], [16]. The receiver circuit converts the RF power to DC voltage, then uses a boost converter to get a high voltage that can be regulated and supply the biomedical device.

Implantable medical devices encounter various real-world challenges that affect their development and implementation. Here are some critical issues:

- Biocompatibility: It's important to make sure that the materials utilized in implants don't react negatively with the body[17].
- Power Supply: One of the biggest challenges is offering a dependable and durable power source[18].
- Biodegradability: Research is beginning to focus on creating materials for temporary implants that can safely break down in the body without harming it[18].
- Miniaturization: The process of shrinking equipment to a size that allows for painless implantation[18].

Despite facing numerous challenges, researchers managed to develop and implement the concept, whether at the circuit level as RF-DC rectifiers[19], [20] or at the implanted device level[21], [22].

In this paper, a high-efficiency RF-to-DC rectifier is being proposed. This paper is organized as follows. Section 2 gives a brief overview of RF-DC rectifier circuits and the techniques used. Section 3 discusses threshold voltage reduction. Section 4 provides the proposed rectifier circuit description. Section 5 shows and discusses the obtained results while the conclusion is driven in Section 6.

2. RF-to-DC Rectifier Circuit

RF-to-DC Rectifier is considered the backbone of the WPT system receivers. Decades ago, RF-to-DC rectifiers were implemented using PN-junctions building the diode bridge rectifier. These rectifiers were less efficient due to the diode built-in potential. Recently, diode-connected devices of MOSFETs played the role of acting as rectifying devices to implement high-efficiency RF-to-DC rectifiers [23]. MOSFET requires threshold voltages (Vth) to switch ON. Although the threshold voltage of MOSFETs (Vth) is less than the PN-junctions turning ON voltage (VD_{ON}), it is still comparable to the weak power input from the WPT system. As a result, some rectifiers utilized Schottky diodes due to their lower threshold voltage compared to PN-junction diodes and diode-connected devices [24], [25]. However, due to production constraints, Schottky diodes are not widely available in conventional CMOS technologies.

There are various CMOS rectifier topologies. The conventional CMOS rectifier is based on the Dickson voltage doubler shown in Fig. 4, which is designed with a series of two NMOS transistors. Each device operates in a half cycle of the RF signal [23], [26]. This circuit seems to double the input voltage, but it also shows a voltage drop that can be as high as twice Vth. Additionally, if voltage doubling is insufficient to reach the necessary output voltage levels, multiple elementary rectifying stages can be cascaded. Fig. 5 shows the NMOS bridge rectifier with differential driving requires the input voltage across the rectifiers to be at least twice the threshold voltage for proper rectification. This design can function even at low input power levels using zero-threshold voltage transistors [23]. A detailed review of different rectifier topologies can be found in [27].

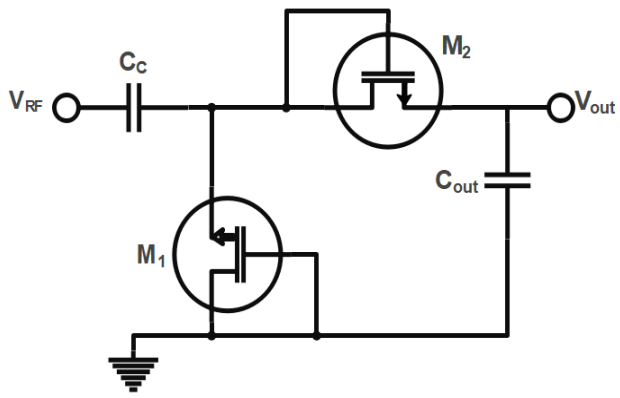

Fig. 4: Conventional CMOS rectifier.

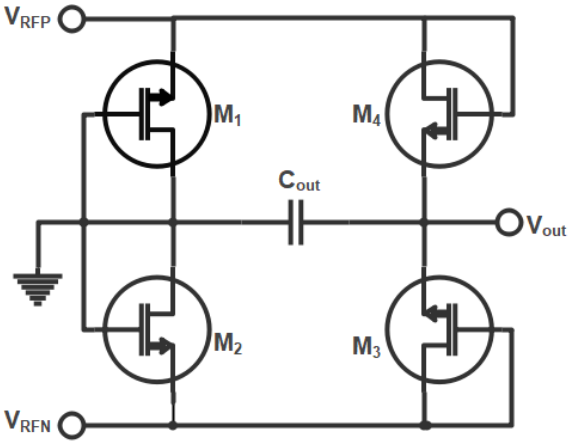

Fig. 5: NMOS bridge rectifier.

Fig. 6 shows a cross-coupled rectifier circuit. It is mainly designed to eliminate the problem of the threshold voltages (Vth) drop on the rectifying transistors (M_{N1}, M_{N2}, M_{P1}, and M_{P2}) of the circuit. This would maximize the rectifier PCE. The differential signals (V_{RFP} and V_{RFN}) change dynamically and switch the rectifying devices ON and OFF. In the positive half cycle (V_{RFP} is positive and V_{RFN} is negative), and when the voltage V_{RFP} is higher than the V_{thN}, M_{N2} conducts at the same time V_{RFN} higher than V_{thP} (in negative sign) M_{P1} conducts due to the V_{SG} overcoming its threshold voltage, while M_{N1} and M_{P2} are OFF and

vice-versa in the negative half cycle. However, the input power levels (P_{IN}) impact its PCE performance the most [28].

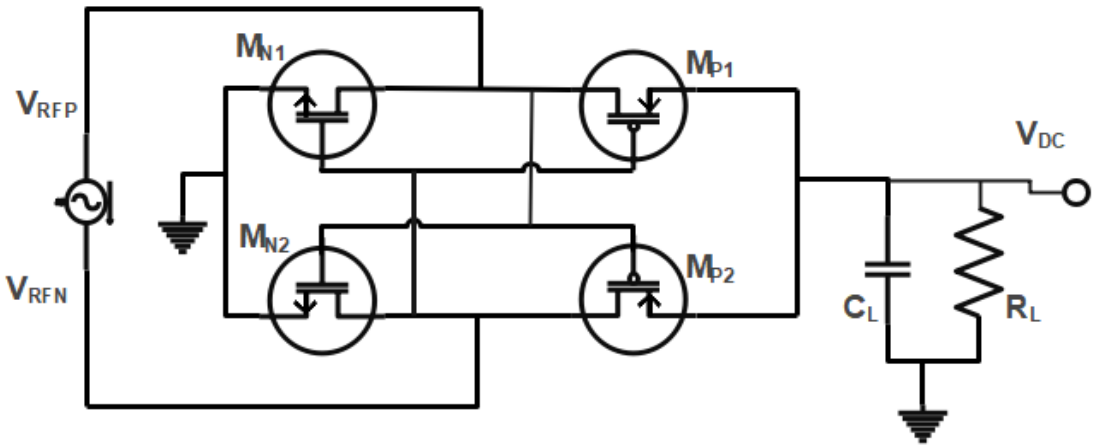

Fig. 6: Conventional cross-coupled rectifier circuit.

In the energy-harvesting wireless power transfer systems, the power delivered to the receiver is too weak. This power needs special techniques to be rectified with minimum power consumption and leakage current [27]
In this study[29], the authors offer a rectifier with input power dependency. Selectively controls the conduction of rectifying transistors using a variable bia sing approach. The "Double-Sided Architecture" technique uses feedback diodes on the MOSFET devices connected to the output to minimize the leakage current in cases of high output voltage. This technique achieves 66% PCE at -18.2dBm input power. For the enhancement of the RF-to-DC rectifier, Maximum Power Point Tracking (MPPT) was presented in [30], which operates in 868 MHZ ISM band. The MPPT technique is usually used for energy harvesting systems to maximize the input power range at which the efficiency is high. This paper experimentally measured 55% PCE @-12.5dBm and 45% PCE @-20dBm.

3. Threshold Voltage Reduction

The traditional cross-coupled circuit - shown in Fig. 6 - does not pass currents to the load (does not rectify the input RF signal to DC voltage) unless the input voltage exceeds the threshold voltage of the device. This would represent an obstacle in the case of small voltages (weak power values), so many research papers turned to research techniques to reduce devices threshold voltages or to compensate these voltages using some external circuits. In [31], a self-biased cross-coupled differential CMOS rectifier with improved efficiency across a larger input range was developed. Threshold voltage compensation was suggested in [32] by using the DC output voltage and the input RF power to cancel the Vth effect. Static Vth-drop compensation (SVC), whose compensation voltage remains constant over time, is an additional threshold compensation method [18]. The rectifier's PCE deteriorates because of the static voltage, which creates a continuous current path and static power usage [33]. The above-mentioned problem is solved in [34] by using dynamic

threshold compensation voltage, which generates the compensation voltage only when needed. For implantable devices that require low input power for RF wireless energy harvesting, a novel differential drive CMOS rectifier topology has been developed in [35]. Using an external bootstrapping circuit and gate biasing of specific MOS switches implement a dynamic threshold compensation mechanism [36].

4. Proposed Rectifier Circuit

4.1. Concept of Clamper Circuit

The proposed circuit is based mainly on the concept of the clamper circuit, which is meant to add a DC level (+ive or -ive) to the input voltage before arriving at the gates of the device. The operation of the clamper circuit is based mainly on a capacitor and a diode (diode-connected PMOS) as shown in Fig. 7 at the positive half-cycle and when the input voltage is a little higher than the Vth of the PMOS (M_P) or when ($V_S>V_G+V_{thP}$), the diode will conduct and can be modeled as an equivalent small on-resistance. At the same time, the capacitor (C_B) starts to charge through the resistor of the diode-connected device in the direction shown. Taking into consideration the time constant of the clamper circuit is about ($C*R_{on}$) which is much greater than the period of the input signal while R_{on}, represents the rectifier device on-resistance. In this circuit, the capacitor acts like a constant DC voltage, so the output voltage is given by ($V_{in}–V_C$).

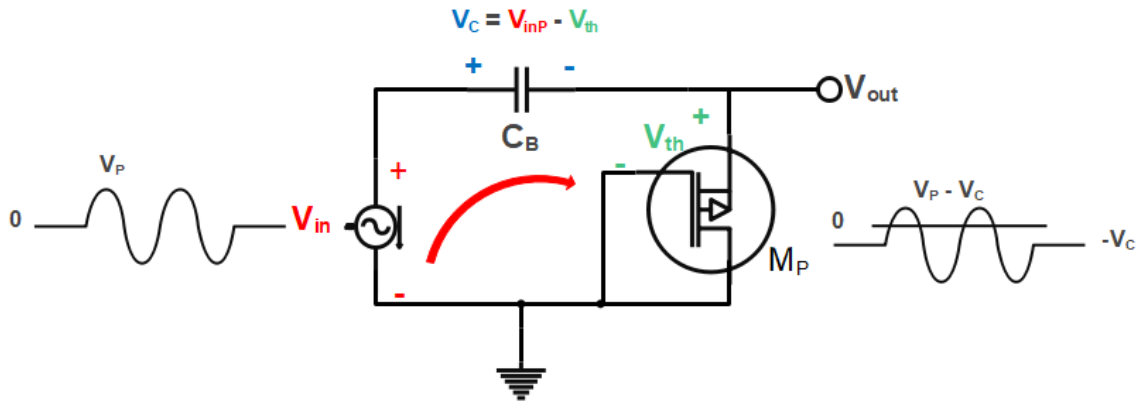

Fig. 7: Negative clamper circuit

4.2. Fully Bootstrap Circuit Operation in the conventional cross-coupled rectifier, the MOSFETs don't switch on until the RF signal exceeds the threshold voltage of the devices. So, we can't have high PCE at low input RF signals. The proposed circuit uses the bootstrapping circuit (clamper circuit) to compensate threshold voltages of the devices, instead of using the RF input voltage to bias the devices. This paper utilizes a bootstrap circuit to compensate for the threshold voltage of the devices. It achieves this by elevating the gate voltage of the NMOS devices using positive DC voltage and reducing the gate voltage of the PMOS devices using negative DC voltage. By this approach, the transistors can conduct faster, resulting in improved power conversion efficiency (PCE) at low input RF power levels.

The fully bootstrap circuit is shown in Fig. 8. The circuit consists of four main rectifier devices M_{N1}, M_{N2}, M_{P1}, and M_{P2}, and four bootstrapping circuits (drawn in blue) to bias the main devices. Positive clamper circuit is used for NMOS gates biasing and negative clamper circuit is used for the PMOS gates biasing.

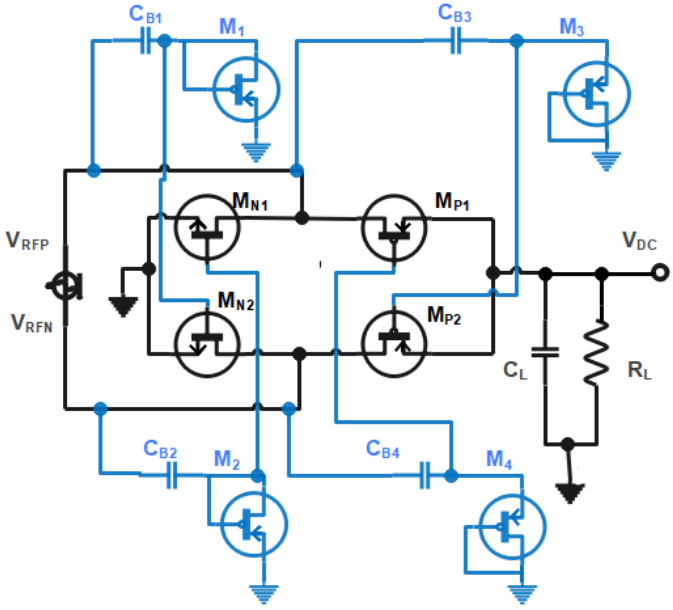

Fig. 8: The proposed fully bootstrapped circuit.

Fig. 7 shows the state of each device in the circuit whether it is on or off in both half cycles. In the positive half cycle Fig.9 (a), the bootstrapping capacitor C_B2 starts to charge through the diode-connected transistor (DCT) M_2. The capacitor C_B3 charges through the DCT M_3 so the bootstrapping capacitor's voltages are given by (1), and (2) respectively: -

$$V_{C_B2} = V_{Peak} - V_{DS(M2)} \quad (1)$$

$$V_{C_B3} = V_{Peak} - V_{SD(M3)} \quad (2)$$

In the negative half cycle Fig. 9 (b), the bootstrapping capacitor C_B1 starts to charge through the diode-connected transistor (DCT) M_4. The capacitor C_B4 charges through the DCT M_4 so the bootstrapping capacitor's voltages are given by (3) and (4) respectively: -

$$V_{C_B1} = V_{Peak} - V_{DS(M1)} \quad (3)$$

$$V_{C_B4} = V_{Peak} - V_{SD(M4)} \quad (4)$$

At steady state, we have constant DC voltage across the capacitors which are used to compensate for the MOSFETs threshold voltages, Fig. 8 shows the gate voltages of NMOS (V_{GN}) and PMOS (V_{GP}) and the input peak voltage (the gate voltage of the traditional cross-coupled gates), the voltages of the gate for both NMOS devices and PMOS devices are given by (5) and (6) respectively.

$$V_{GN1,2} = V_{Peak} + V_{C_B2,1} \quad (5)$$

$$V_{GP1,2} = V_{Peak} - V_{C_B4,3} \quad (6)$$

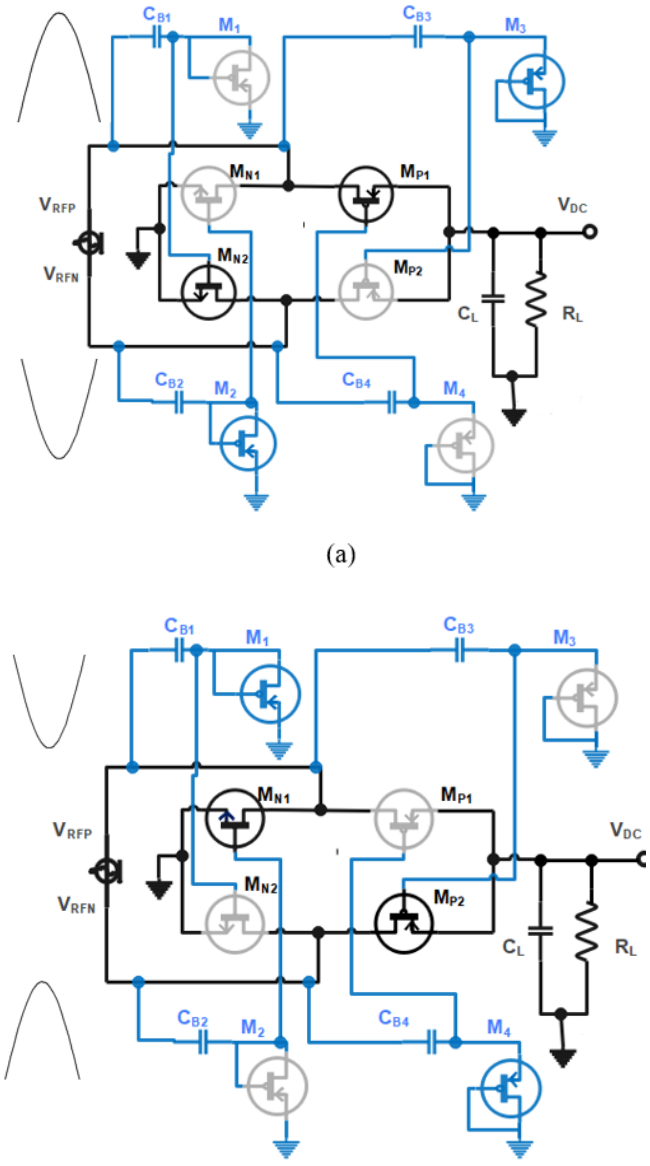

Fig. 9: Operation of the proposed rectifier during (a) positive half cycle and (b) negative half cycle.

The simulation results of the suggested bootstrapping circuits are shown in Fig. 10, whereas the NMOS and PMOS devices gate voltages are compared to the input voltage. The gate voltages variations of two rectifying transistors, M_N2 and M_P2, are displayed over time. The suggested rectifier conducts with a lower input voltage because the gate bias voltage of the PMOS transistor (V_{GP}) becomes more negative, and V_{GN} becomes more positive than the comparable value of the conventional rectifier [28]. Consequently, the suggested rectifier can achieve a greater PCE at low RF input power.

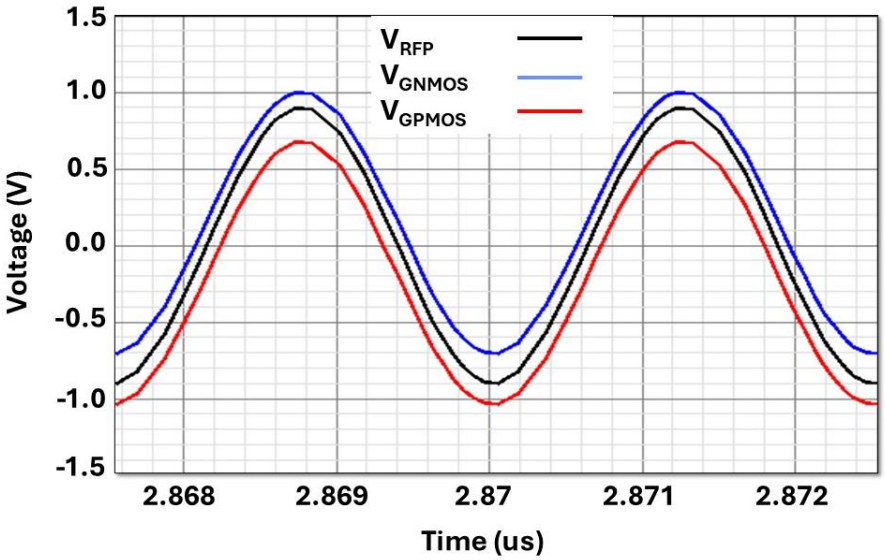

Fig. 10: NMOS and PMOS gate voltages compared to the input voltage.

5. Results and Discussion

The proposed circuit is designed and simulated using Agilent Advanced Design System (ADS) in TSMC 180nm CMOS technology. Electromagnetic simulation is verified using a cadence design environment. The load resistor and capacitor were varied to enhance the performance of the proposed fully bootstrapped RF-to-DC rectifier. The simulation results are given below. The RF-to-DC rectifier power conversion efficiency (PCE) and voltage conversion ratio (VCR) are given by (7) and (8) respectively.

$$\boldsymbol{PCE} = \frac{\boldsymbol{P_{out}}}{\boldsymbol{P_{in}}}(\%) \tag{7}$$

where.

$$\boldsymbol{P_{out}} = \frac{\boldsymbol{1}}{\boldsymbol{nT}} \int_{\boldsymbol{0}}^{\boldsymbol{nT}} \frac{(\boldsymbol{V_{out}(t)})^{\boldsymbol{2}}}{\boldsymbol{R_L}}$$

$$\boldsymbol{P_{in}} = \frac{\boldsymbol{1}}{\boldsymbol{nT}} \int_{\boldsymbol{0}}^{\boldsymbol{nT}} \boldsymbol{V_{in}(t) I_{in}(t)}$$

$$\boldsymbol{VCR} = \frac{\boldsymbol{V_{DC}}}{\boldsymbol{V_{peak}}}(\%) \tag{8}$$

where P_{out} represents the DC output power, P_{in} represents the RF-to-DC rectifier AC input power, R_L is the load resistive portion, T presents the RF input signal period, n is the number of RF input signal considered cycles, V_{DC} is the rectifier DC output voltage, and V_{peak} is the input signal peak value. The transient behavior of the proposed rectifier is simulated. Simulation results of the DC output voltage are shown in Fig. 11. The Settling time of the transient output signal is about 20ns. Fig. 12 shows the DC obtained output voltage in

comparison to the input voltage (in red, V_{peak} =1V). Fig. 13 shows the results of the PCE of the proposed rectifier at various values of the load resistance, and it shows that the efficiency was maximized at R_L=12kΩ. The load resistor affects the PCE, where we can achieve PCE above 70% at the range of 4KΩ to 40KΩ load resistance.

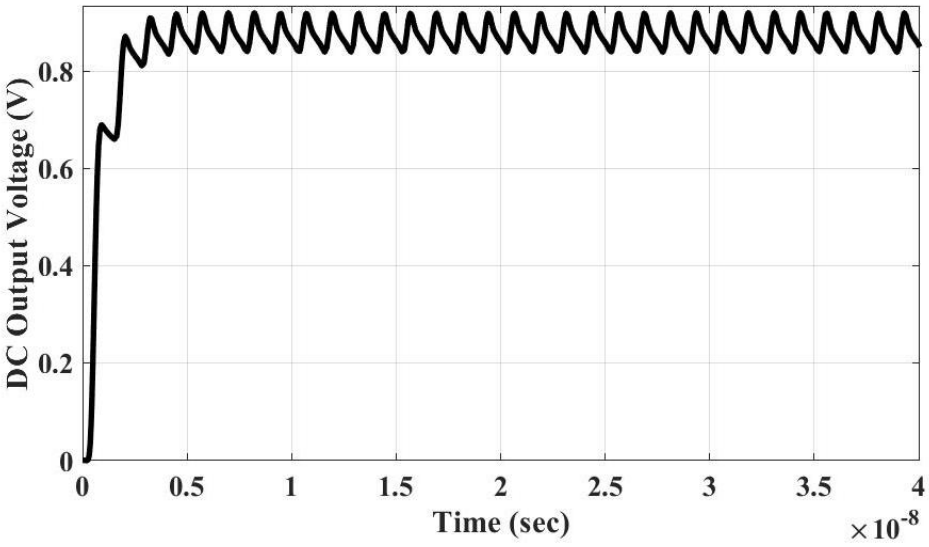

Fig. 11: The output of the circuit (DC voltage).

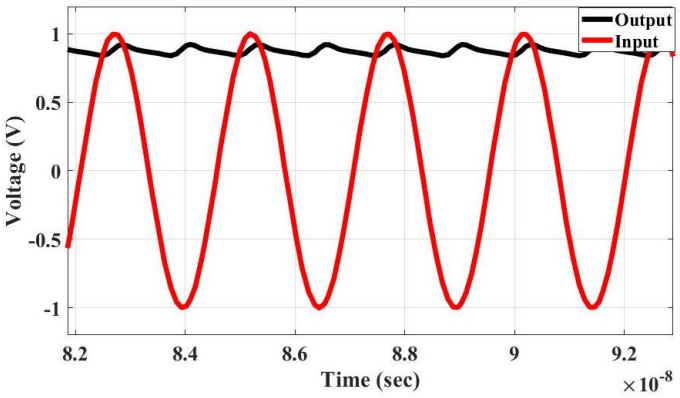

Fig. 12: Output and input voltages at peak V_{inP}=1V

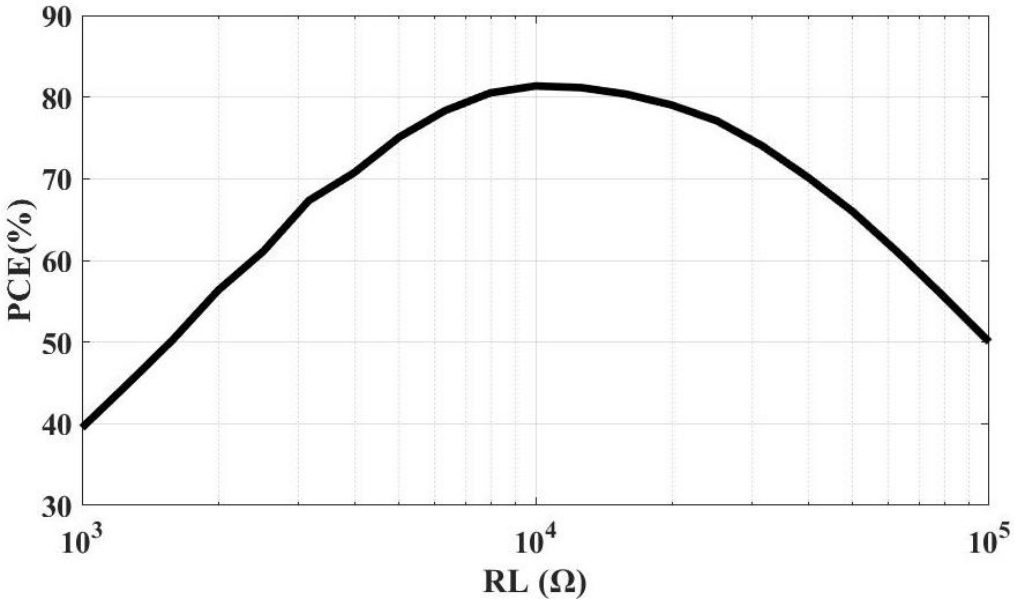

Fig. 13: PCE at various loads from 1KΩ to 100KΩ.

The PCE is simulated considering the RF input power. Simulation results are shown in Fig. 14. The PCE is being increased with the increase of the input RF power. It achieves its maximum of 80% at an input RF power of -12.4dBm. Several factors contribute to the decrease in efficiency after reaching its maximum value. These factors include the increase in conduction losses, the effects of parasitic capacitances, the non-ideal behavior of NMOS and PMOS devices at higher power levels. Pushing the MOSFET devices operating points (Q) from the sub-threshold region - at low input power- to the linear region -at increased input RF power- increases the device dissipated power. These lead to a reduction in overall efficiency [37]. Fig. 15 shows the VCR which is maximized to a value of 87% at an input RF power of -10.76 dBm.

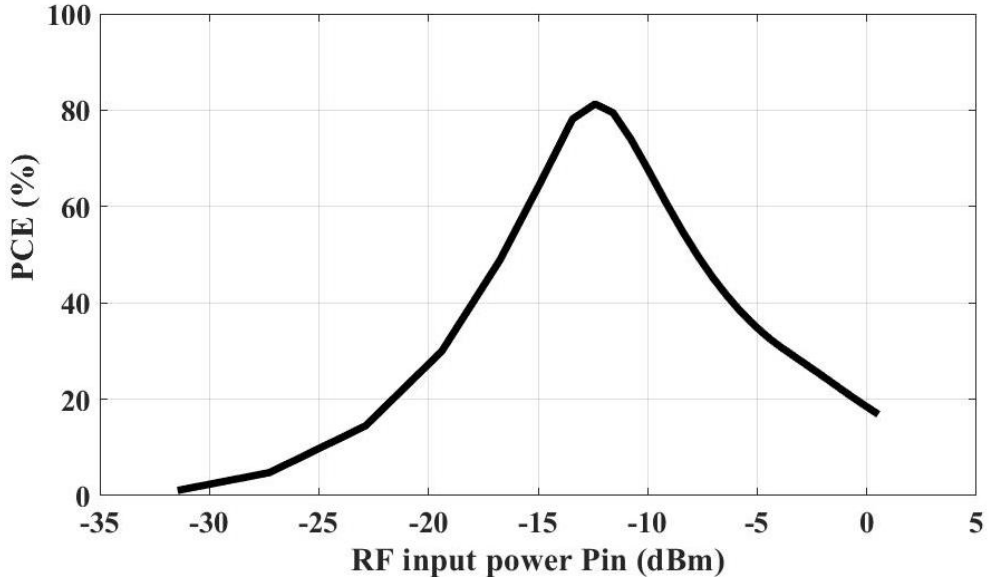

Fig. 14: PCE of the proposed rectifier circuit.

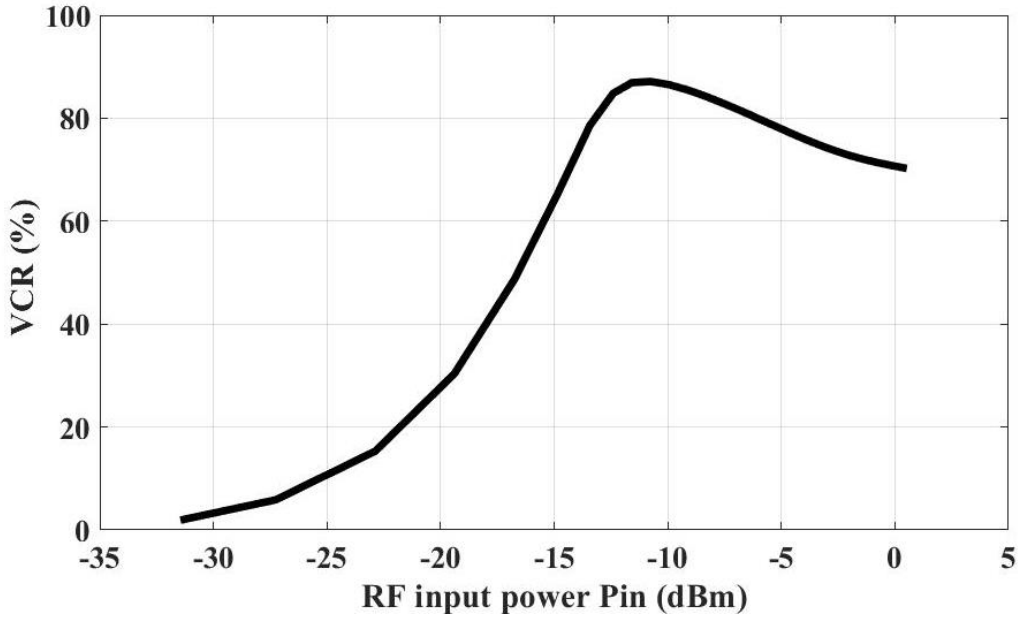

Fig.15: VCR of the proposed rectifier circuit.

Fig.16 shows the dependency of the proposed rectifier PCE on the frequency of the input RF power. As shown in the figure, the efficiency of the circuit is high over a wide range of frequencies, but the presented rectifier is designed to operate over this ISM frequency band

(402 MHz). The proposed rectifier is also simulated at another frequency at an ISM-band frequency of 434MHz. Fig. 17 shows the comparison between the obtained PCE at 402 MHz and at 432 MHz The results are concise to each other means the proposed rectifier circuit behaves the same at a wide range of frequencies at ISM-band of frequencies. Table 1 lists the presented rectifier components' values and parameters while Table 2 summarizes the performance of the RF-to-DC rectifier in comparison to recently published counterparts.

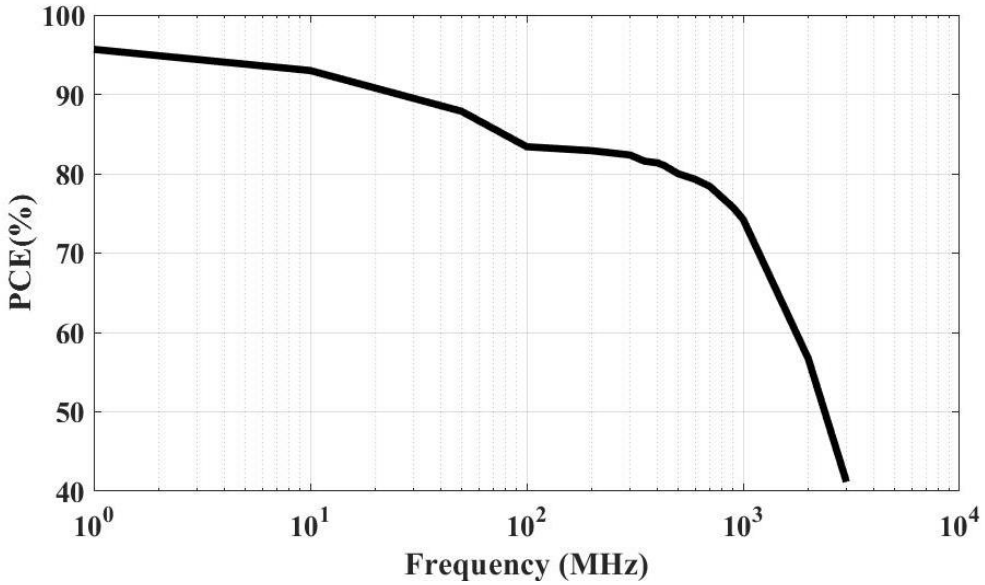

Fig. 16: PCE at various frequencies of input RF signal.

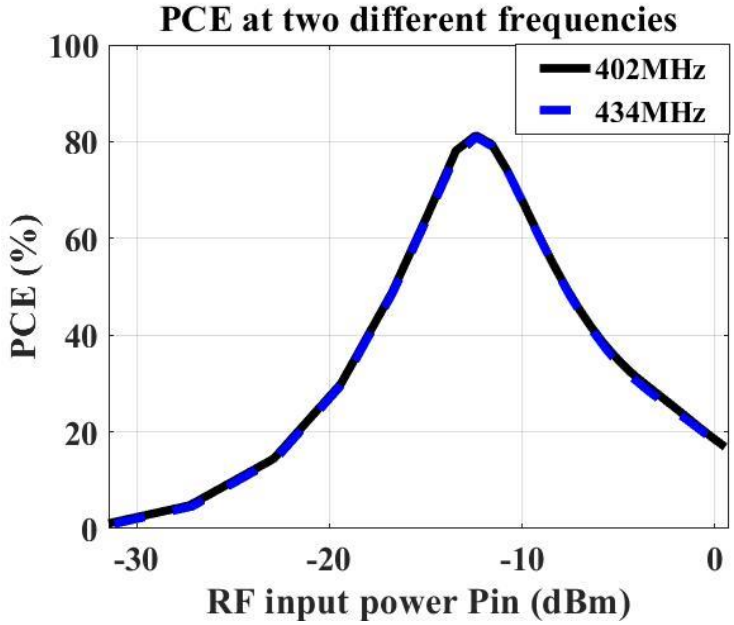

Fig. 17: The simulation results of PCE at two different frequencies.

Table 1: Circuit components values and devices parameters.

Component	M_N1, M_N2^*	M_P1, M_P2^*	M1-M4*	C_{B1}-C_{B4}	C_L	R_L
Value	(6 x20)/0.4	(7x20)/0.3	(1.5x1)/0.5	6pF	1pF	12KΩ

*Sizing of devices is (W x N_F)/L [µm], where W is the device width, L is the device length, and N_F is the number of fingers.

Table 2: Performance summary and comparison with recently published counterparts.

	[28] 2009	[38] 2012	[35] 2016	[39] 2023	[40] 2023	[34] 2023	**This Work**	
Process[nm]	180	180	180	65	180	180	**180**	**180**
Freq [MHz]	953	10	402	200	434	433.92	**434**	**402**
Topology	DD[1]	BS[2]	CC[3]	FCC[4]	BS[2]	BS[2]	**FBS[5]**	**FBS[5]**
Application	UHF RFIDs	WPT[6]	UHF	WPT[6]	WPT[6]	WPT[6]	**WPT[6]**	**WPT[6]**
No of stages	1	1	1	3	1	1	**1**	**1**
R_L [KΩ]	10	2	10	3	3	3	**١٢**	**12**
P_{in} range [dBm]	-30 to 0	N/A*	-23 to -7	-4 to 7	-6 to 6	-6 to10	**-30 to 0**	**-30 to 0**
PCE_{max} [%]	67.5	71	75	70.3	71	68.5	**80.85**	**81.3**
P_{in} [dBm] @ PCE_{max}	-12.5	N/A*	-15.4	7	3	0	**-12.8**	**-12.4**
DR [dB] @ PCE	17 @ >30%**	N/A*	12 @ >30%**	12 @ >30%**	15 @ >30%	>16 @ >30%	**15.4 @ >30%**	**15.7 @ >30%**
VCR_{max} [%]	N/A*	75% @V_{RFP} =1V ***	83.9 @V_{RFP} =0.5V	75% @V_{RFP} =1V***	91% @V_{RFP} =2V	85% @V_{RFP} =2V	**87.14% @V_{RFP} =1V**	**87% @V_{RFP} =1V**

[1] Differential Drive, [2]Bootstrap, [3] Cross-Coupled, [4] Fully Cross-Coupled, [5] Fully Bootstrap, [6] WPT for implants.
*Not available, **Estimated from the measured PCE graph, ***Estimated from the measured VCR graph

6. Conclusions

This paper presents a high-efficiency rectifier circuit with fully bootstrapped devices. The proposed circuit consists of four main rectifier transistors (diode-connected devices) biased with four clamper circuits to compensate for those devices' threshold voltages. Loaded with C_L of 1pF and R_L of 12kΩ, the circuit was designed and simulated in 180n CMOS process. With an input signal of 402MHz, the proposed RF-to-DC rectifier has a maximum PCE of 81.3% and a VCR of 85% at an input RF power of -12.4dBm. This rectifier achieves a relatively wide dynamic range of 15.7dB (PCE > 30%). The proposed rectifier has superior performance over a wide range of RF frequencies.

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