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# On the Use of Forward Body Biasing Technique for Low Power Ultra-Wideband Low Noise Amplifiers Design and Implementation

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**Keywords**
Cascode, Current Reuse, Forward Body Biasing, (FBB), Low power, Low Noise Amplifier (LNA), Ultra-wideband (UWB)

**Abstract:** This paper discusses the utilization of forward body biasing (FBB) technique for low power low noise amplifier (LNA) design. Two low power wideband LNAs utilizing current reuse with FBB technique are being presented. LNA1 is a cascode (common gate followed by common source) LNA while LNA2 is implemented as a current reuse (common source followed by common source). FBB is used for presented LNAs input gates' transconductance boosting. LNA1 has a minimum post layout noise of 3.9 dB and a maximum gain of 12.5 dB. Its circuit current that derived from 0.65 voltage supply is only 1.68 mA. LNA2 achieves a high post-layout gain. Its maximum value is 13.6dB. It has a flattened post-layout noise figure with a minimum value of 3.19 dB. It is powered from a 0.615V and drives a current of 10.7 mA. With a dissipated power of 1.09 mW and 6.58 mW for LNA1 and LNA2, respectively, both LNAs have good isolation performance. LNA1 and LNA2 have output and input matching impedance over the ultra-wideband (UWB) frequency range of interest (3.1~10.6 GHz). These low power ultra-wideband LNAs are designed and simulated in CMOS 130nm process.

## 1. Introduction

Ultra-wideband (UWB) is a wireless communication technology that uses a very low power level to transmit data over a wide range of frequencies. It is also known as impulse radio, because it uses short pulses of energy to transmit data. UWB has many advantages over other wireless technologies, including high data rates, low power consumption, and the ability to penetrate walls and other obstacles [1]. UWB was first developed in the 1960s for military applications such as radar and communications. However, it was not until the 1990s that UWB began to be used for commercial applications. Today, UWB is used in a variety of applications, including wireless USB, location tracking, and medical imaging. [1], [2].

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Another advantage of UWB is its low power consumption. Because UWB uses short pulses of energy to transmit data, it requires much less power than other wireless technologies. This makes it ideal for battery-powered devices such as smartphones or wearables [3]. A low noise amplifier (LNA) is an essential stage in modern communication systems, particularly in wireless applications. It plays a crucial role in amplifying weak signals while introducing minimal noise to the system. The primary objective of an LNA is to improve the signal-to-noise ratio (SNR), ensuring that the received signal can be accurately detected and processed.

One of the main challenges in wireless communication is dealing with weak signals that are susceptible to noise interference. As signals travel through various mediums, they tend to weaken, making it difficult for receivers to detect and interpret them accurately. This is where LNAs come into play, as they provide the necessary amplification to boost these weak signals without adding significant noise. The key characteristic of an LNA is its low noise figure (NF), which quantifies the amount of additional noise introduced by the amplifier. A lower NF indicates a better LNA performance, as it means that the amplifier adds less noise to the received signal. Achieving a low NF requires careful design considerations and optimization techniques. [2].

In conclusion, low noise amplifiers play a vital role in modern communication systems by enhancing weak signals while keeping additional noise at a minimum level. Their ability to improve SNR ensures accurate detection and processing of received signals across various applications ranging from wireless communication systems to medical devices and scientific instruments. In addition, the power dissipation performance of LNA is one of the important factors that we should keep in mind when designing a good RF receiver chain in any portable application. Throughout this paper, two LNA designs are being presented having efficient enhancement of power dissipation performance.

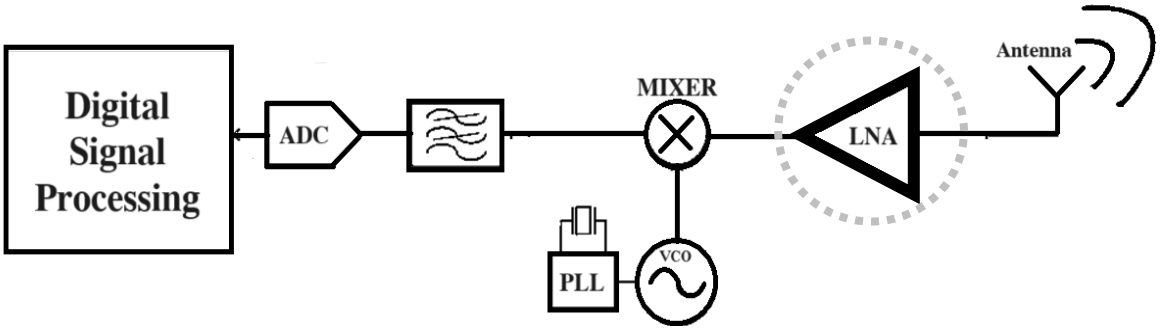


Fig. 1. RF receiver chain

Many low voltage designs were proposed in [5]-[11]. In [5] a self-resonant transformer matching is presented, but it suffers from large die area, small bandwidth, and higher noise figure. RLC coupling technique is used to enhance the circuit matching proposed in [6], but it dissipates high power from its voltage supply. A high gain over a wide band of spectrum was achieved by designing three cascaded stages LNA presented in [7]. This was achieved

by shunt-series boosting mechanism, but it drains very high current from its power supply and its power dissipation is 45mW. In [8] a good input and output circuit matching was achieved, but it has a high noise performance. Cascaded Common Source stages were presented in [9], but it has a high derived current to enhance the performance of circuit noise. A forward body biasing technique with narrow band LNA is presented in [10]. It consumes low power and has a high gain with good input and output impedance matching, but this degrades the noise performance of the presented LNA. High and broaden gain LNA is presented in [11]. This LNA can be considered an ultra-low power LNA as it dissipates 2 mW only of power. But it cannot utilize deep output impedance matching.

## 2. Forward Body-Biasing Technique

The basic principle behind forward body biasing is that it can increase the drive current of a transistor by reducing its threshold voltage. The threshold voltage is the minimum voltage required to turn on a transistor, and it is typically set by doping concentration in the channel region. By applying a positive voltage to the substrate, as shown in Fig. 1, which is typically connected to ground, the doping concentration in the channel region can be effectively reduced, lowering the threshold voltage. This reduction in threshold voltage can have several benefits for CMOS circuits. First, it can increase their speed by allowing them to switch faster. This is because a lower threshold voltage means that less charge needs to be accumulated in the channel region before the transistor turns on. Second, it can reduce their power consumption by allowing them to operate at lower voltages. This is because a lower threshold voltage means that less voltage needs to be applied across the transistor to turn it on [8]. Another advantage of body biasing is that it can compensate for process variations that occur during manufacturing. Process variations can cause variations in threshold voltage between transistors on the same chip, which can lead to timing errors or other performance issues. By using body biasing, designers can adjust the threshold voltages of individual transistors to compensate for these variations and improve overall circuit performance.

In contrast to the other three terminals, the body terminal is less commonly employed in MOS transistors. Several designs simply assume that the body terminal is connected to the source terminal (GND in NMOS devices and VDD in PMOS devices). The p-type substrate has two connections with the n-type sections of source and drain. Fig. 2(a) shows the structure of the NMOS transistor illustrating these back-to-back diodes. These unneeded diodes are disregarded for metal-oxide-semiconductor (MOS) transistors since they are commonly biased in reverse conditions to reduce their impact on the performance of metal-oxide-semiconductor transistors. However, if the body voltage is adjusted to a different value from that of the source, the biasing of substrate terminal affects the transistor's operation parameters. In general, the substrate terminal behaves as a "second gate" for

metal-oxide-semiconductor devices. Hence, it is called a “back-gate” terminal [8]. While forward bias these bulk-source junction, a resistive current blockage must be inserted in series to MOS body. This prevents all dc or ac current passing and saves the MOS structure unaltered.

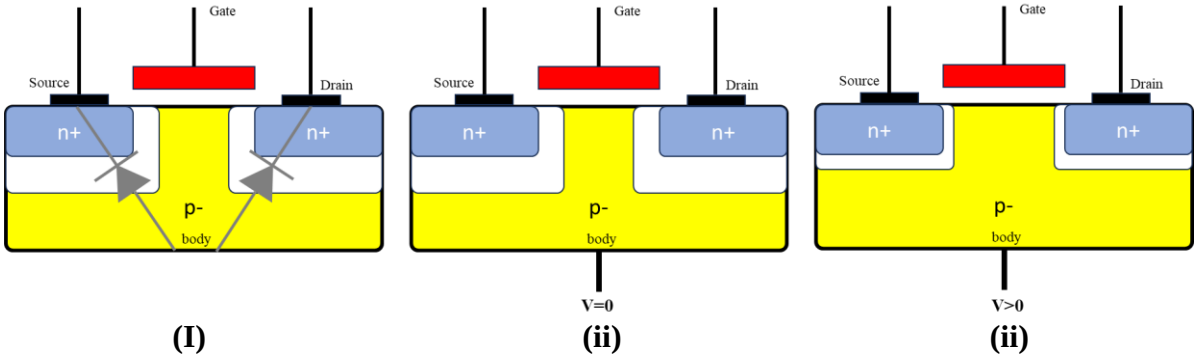


Fig. 2. MOS structure (i) parasitic diodes (ii) zero body biasing (ii) forward body biasing

The depletion area in the MOS transistor body will decrease with the gate terminal voltage if its value is positive. Thus, the channel inversion phenomena occurred at a lower threshold voltage. To lessen the impact of the reverse biasing of body voltage, a gate with a higher potential would be required for strong inversion and channel construction if the body voltage turned negative, and vice versa. This is indicated by the dependency of the gate-source threshold voltage on the source-bulk voltage difference described by (1) [4]: -

$$\boldsymbol{V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\emptyset_f| + V_{SB}} - \sqrt{|2\emptyset_f|}\right)} \quad (1)$$

Where $V_{TH0}$: defined as threshold voltage at zero body voltage, $\gamma$: defined as the process factor and sometimes called as body effect parameter, $\phi_f$: defined as work function of semiconductor, and $V_{SB}$ defined as source-bulk voltage.

By using the body terminal, gain boosting can be done. To guarantee the parasitic diodes are OFF, a weak forward biasing technique was suggested. In conclusion, the MOS transistor gain will increase when the bulk terminal is weakly forward biased. This improves the transconductance performance of the NMOS transistor. The non-zero body potential boosts the device bulk transconductance ($g_{mb}$), as indicated by (2) and (3) [4]. So, the device total transconductance ($GMT$) is given by: -

$$g_{mT} = g_m + g_{mb} \quad (2)$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{SB}} = g_m \cdot \frac{\gamma}{2\sqrt{|2\emptyset_f| + V_{SB}}} = \eta g_m \quad (3)$$

### 2.1. Gain Boosting using Forward Body-Biasing

As shown in Fig. 3, the bulk transconductance $g_{mb}$ for the input NMOS gate of LNA1 "M1" increases with the increase of bulk potential in respect to source. It reaches a maximum value of 4.8 mS at the bulk-source potential mid-range. It is also noted that bulk transconductance $g_{mb}$ decays with the further increase in bulk-source voltage. Hence, there is an optimum range of bulk potential difference to apply for $g_{mb}$ boosting. Similarly, M1 input transistor in LNA2 design has the same phenomena with slight difference in range at which $g_{mb}$ is maximum.

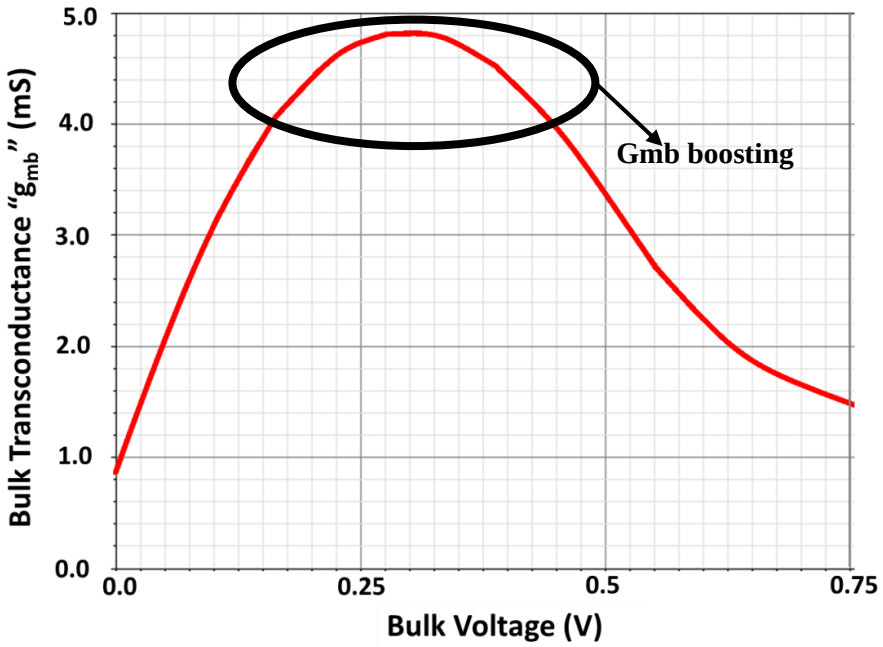


Fig. 3. Bulk transconductance ($g_{mb}$) vs. bulk potential difference ($V_{bs}$)

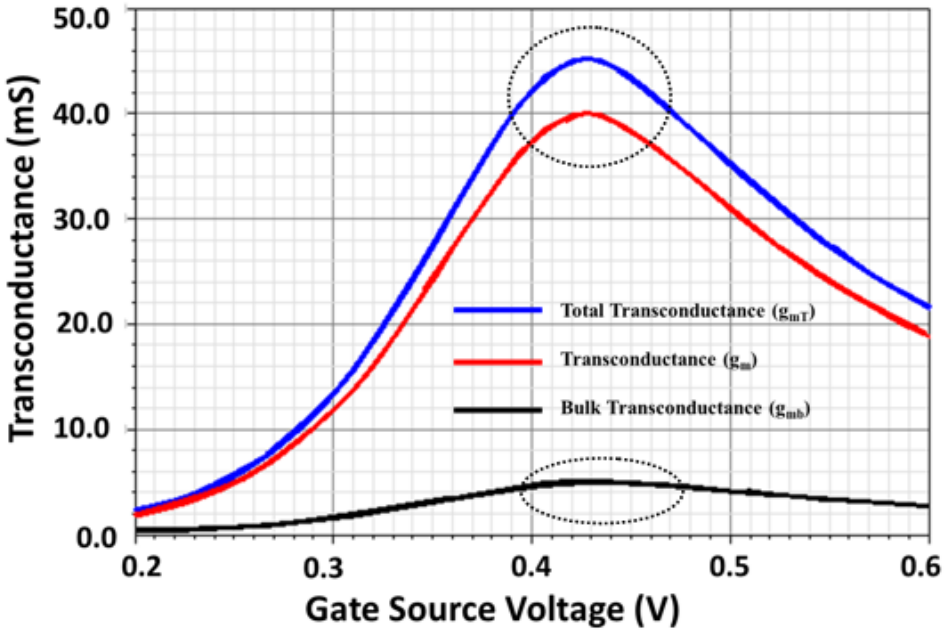


Fig. 4. Bulk trans conductance ($g_{mb}$), trans conductance ($g_m$) and total trans conductance ($g_{mT}$) of $M_1$ in LNA1 vs. gate-source voltage ($V_{GS}$) at ($V_b$=290 mV).

In Addition, forward body-biasing (FBB) helps LNA to drive less drain current and achieve an enhanced gain compared to the gain achieved with no utilization of FBB. This phenomenon is described as follows. Referring to Fig. 4, if $g_m$ is desired to be increased by factor of ~5 mS, we need to increase the drain current 1.7 times, refer to Eq. 4, to get the same effect of gain boosting by using forward body-biasing technique. In other words, the FBB technique saves about 30% of power consumption that will be used by increasing the drain current to get the same gain boosting level. In eq. (4), the relation between transconductance and the drain current is defined [4]

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_{TH}} \tag{4}$$

Where $g_m$: is CMOS transistor transconductance, $I_D$: is the drain current, $V_{GS}$: is the gate-source voltage, $\mu_n$: is electron permeability, $C_{ox}$: is dioxide capacitance,$\frac{W}{L}$: is the CMOS transistor dimensions aspect ratio, $V_{th}$: is threshold voltage of CMOS transistor.

For consideration of the threshold affected by the variation of the bulk-source potential difference, the threshold voltage dependency on FBB technique was simulated. Simulation results are given by Fig. 5. $V_{TH}$ value decreases with the increase of bulk voltage while the device source is grounded. In addition, it leads to strong inversion and channel formulation at lower values of gate-source voltages ($V_{GS}$). This would boost the device transconductance and induce a non-zero bulk Tran's conductance ($g_{mb}$).

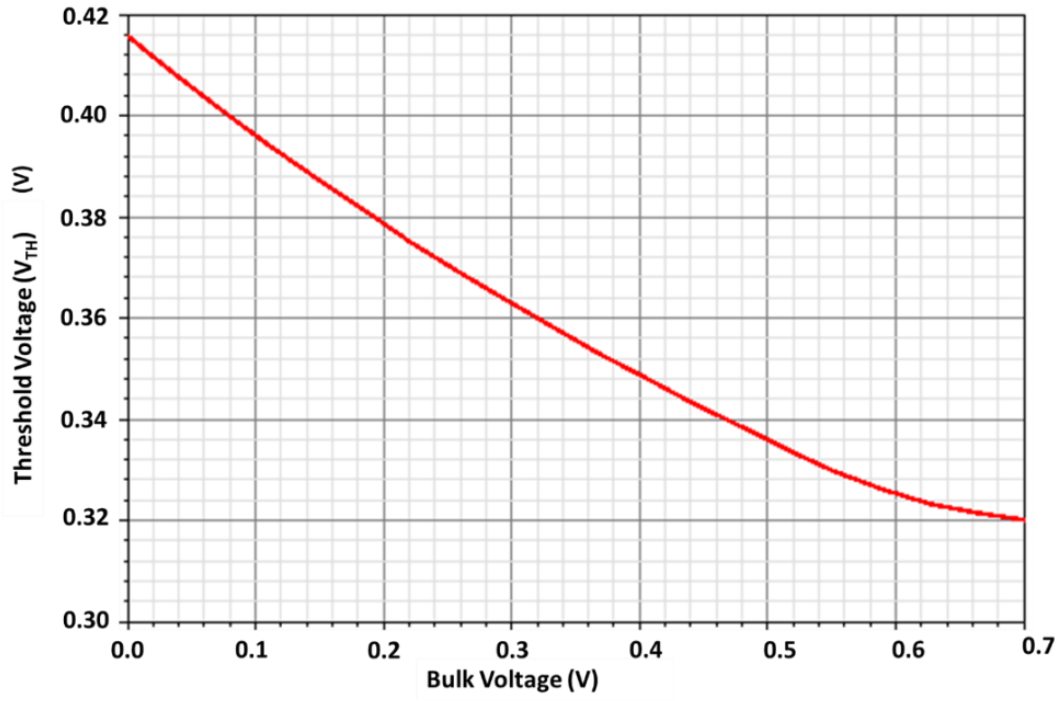


Fig. 5. Threshold voltage vs. bulk voltage of $M_1$ in LNA1 (Vs=0V)

## 3. Circuit Description

In this paper, two designs of LNA using Forward Body-Biasing are presented. The first LNA has a CG-CS topology and is termed LNA1. Secondly, LNA2 has a current reuse CS-CS topology. Both designs are proposed using FBB for performance enhancement and dissipated power minimization.

### 3.1. Common Gate-Common Source Current Reuse Low Noise Amplifier [LNA1]

As shown in Fig. 6, the suggested UWB-LNA scheme employs CG-CS configuration with current reuse. The proposed LNA1 employs current reuse combining a CG topology followed by a CS topology. CG topology plays an important role as input stage for LNA input matching. The output stage is configured as CS. This combination is an effective method for achieving high broaden power gain, and consuming low DC power. This also helps to achieve good wide input and output impedance matching, low noise figure, and a smaller die area [1]. To achieve a wide good input matching through the desired UWB range, a CG input stage is adopted. The CS high gain and good output impedance matching helped improve the whole LNA performance. FBB is used to obtain a wider boosted CG gain. A resistive current blocking path with $R_b=10\ k\Omega$ is inserted to prevent bulk-source diode latch-up. Additionally, by utilizing series gate peaking technique, the overall LNA1 gain was boosted. The inductive-resistive shunt peaking played a crucial role for LNA gain flattening. The equation below describes LNA1 gain factor including input stage overall transconductance ($g_{mT1}$), and the subscript one refers that FBB technique applied to $M_1$ transistor:

$$\boldsymbol{A} = \frac{(\mathbf{1}+\boldsymbol{g_{mT1}r_{o1}})\boldsymbol{g_{m2}}((\boldsymbol{R_{d2}}+j\omega\boldsymbol{L_{d2}})//\boldsymbol{R_{out}})}{(\boldsymbol{r_{o1}}+j\omega\boldsymbol{L_{d1}})j\omega\boldsymbol{C_{gs2}}} \tag{5}$$

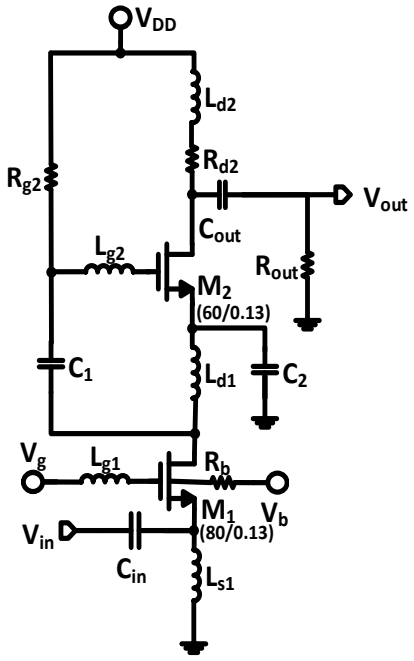


Fig. 6. Schematic circuit of the proposed cascode LNA (LNA1)

FBB increases device transconductance while decreasing the input-referred components of gate thermal and flicker noise [8]. An inter-stage *LC* matching network is used to improve noise immunity and performance, allowing for maximum power transfer [9]. The NF is minimized in this LNA1 design due to effective inter-stage match implementation. To achieve effective output matching, we apply a parallel inductor peaking technique to reduce output return loss. In addition, an output resistance $R_{out}$ was inserted at the output terminal to broaden the bandwidth of output impedance matching. Table 1 lists the values of LNA1 circuit components (transistor dimensions (*W/L*), resistors, inductors and capacitances)

**Table 1:** The Values of Proposed LNA1 (Current Reuse CG-CS) Circuit Components

| | |
|---|---|
| $V_{DD}$ | 650 mV |
| $V_g$ | 430 mV |
| $C_{in}$ | 20.6829 pF |
| $L_{s1}$ | 8.90189 nH |
| $L_{g1}$ | 318.964 pH |
| $C_1$ | 10.3982 pF |
| $M_1$(W/L) | 80u/130n |
| $M_2$(W/L) | 60u/130n |
| $L_{g2}$ | 2.31051 nH |
| $L_{d1}$ | 8.78337 nH |
| $C_2$ | 7.06285 pF |
| $C_{out}$ | 899.947 fF |
| $R_{out}$ | 535.14 kΩ |
| $R_{G2}$ | 40 kΩ |
| $R_{d2}$ | 30 kΩ |
| $L_{d2}$ | 1.2275 nH |
| $R_b$ | 10 kΩ |
| $V_b$ | 290 mV |

### 3.2. Common Source-Common Source Current Reuse Low Noise Amplifier [LNA2]

LNAs that use common source topology have high flatten power gain, good noise and isolation, while utilizing lower power consumption. As shown in Fig. 7, LNA2 employs current reuse common source-common source topology with inductive gate peaking. It also uses shunt capacitive resistive feedback technique to decrease the noise in the circuit. Besides gate peaking which boosts the gain in the high frequency spectrum, it uses shunt peaking technique that has high gain in the low frequencies. This design has good input matching over the wideband range of frequencies, this performance utilized by using the inductive degeneration $L_s$ and gate inductance $L_g$. The input impedance $Z_{in}$ of the circuit is

given by Eq. (6) and (6.1), $\omega_T$ is the current-gain cut off frequency, $g_m$ and $C_{gs}$ are the trans-conductance and the gate-source capacitance of $M_1$ MOS device, respectively.

$$Z_{in} = j\omega\left(L_s + L_g\right) + \frac{1}{j\omega C_{gs}} + \omega_T L_s \quad , \omega_T = \frac{g_m}{C_{gs}} \tag{6}$$

$$Z_{in} = j\omega\left(L_s + L_g\right) + \frac{1}{j\omega C_{gs}} + R_s \tag{6.1}$$

A week feedback circuit ($R_{fb}$, $C_{fb}$) was adopted for gain flattening. This excludes the feedback circuit from contributing to the impedance real portion. In addition, the current path of $C_{fb}$+$R_{fb}$+$L_{d1}$+$C_2$ is considered a high impedance path comparable to $R_s$. Thanks to weak resistive feedback used in LNA2 that has flattened the gain over frequency range of interest. The gain equation of LNA2 design is described in Eq. (7) as follows,

$$\boldsymbol{A = \frac{g_{mT1} \cdot g_{m2}[R_L // (R_{d2} + j\omega L_{d2})][j\omega L_{d1}]}{2\, j\omega C_{gs1}[j\omega(L_{s1} + L_{g1}) + \frac{1}{j\omega C_{gs1}}]}} \tag{7}$$

$$\boldsymbol{g_{mT1} = g_{m1} + g_{mb1}} \tag{8}$$

Where $g_{mT1}$ refers to the total transconductance of $M_1$ transistor in LNA2. Table 2 lists the components' values of LNA2 circuit (transistor dimensions (*W/L*), resistors, inductors and capacitances)

**Table 2:** The Values of Proposed LNA2 (Current Reuse CS-CS) Circuit Components

| | |
|---|---|
| $V_{DD}$ | 615 mV |
| $V_g$ | 400 mV |
| $L_{s1}$ | 208 pH |
| $L_{g1}$ | 539.647 pH |
| $C_{fb}$ | 0.5 pF |
| $R_{fb}$ | 1.5 KΩ |
| $M_1$(W/L) | 140u/130n |
| $M_2$(W/L) | 108u/130n |
| $L_{g2}$ | 1.0629 nH |
| $L_{d1}$ | 16.1432 nH |
| $C_1$ | 8 pF |
| $C_2$ | 8 pF |
| $R_{G1}$ | 30 KΩ |
| $R_{G2}$ | 30 KΩ |
| $R_{d2}$ | 18 Ω |
| $L_{d2}$ | 1.4645 nH |
| $C_{in}$ | 31.8309p F |
| $R_b$ | 10.0002 k |
| $V_b$ | 430mV |

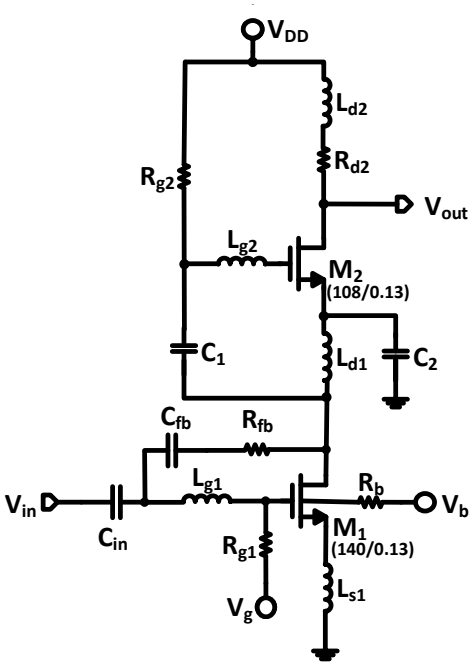


Fig. 7. Schematic circuit of the proposed current reuse LNA (LNA2)

## 4. Results and Discussion

These ultra-wideband LNAs were developed and simulated in CMOS 130nm process. Considering their low DC power consumption, these LNAs with FBB results were verified by electromagnetic simulation after parasitic extraction. The layouts of the proposed LNAs (LNA1 and LNA2) are shown in Fig. 8 and Fig. 9, respectively. LNAs (LNA1 and LNA2) occupy an area of 0.71712 $mm^2$ and 0.499 $mm^2$, respectively.

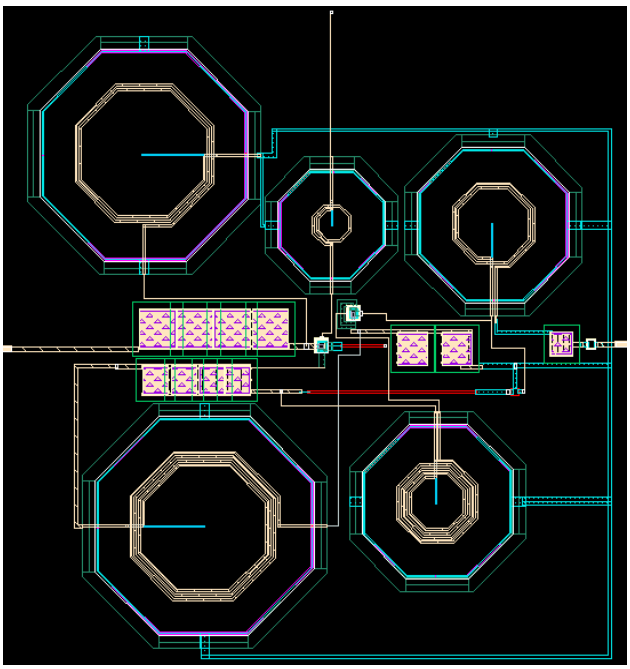

Fig. 8. Layout of LNA1 (830 µm X 864 µm)

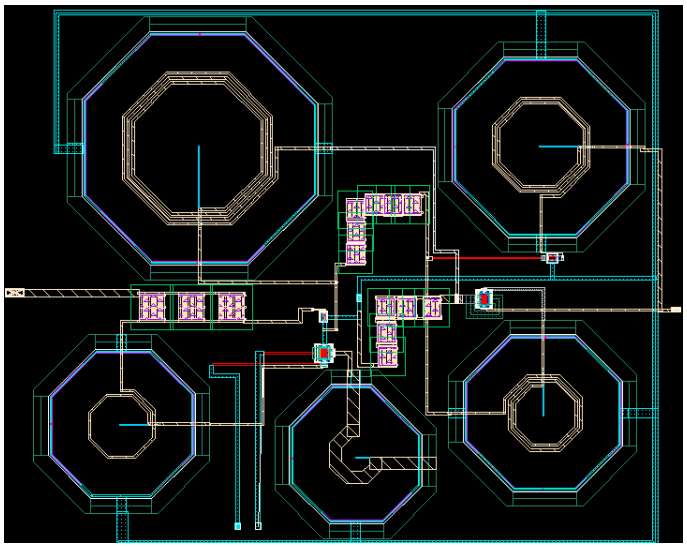

Fig. 9. Layout of LNA2 (763 µm x 655 µm)

## 4.1. Power Gain and Noise Figure

### 4.1.1.LNA1 Gain and NF

The proposed LNA1 has a 9.75±2.75 dB gain over the desired band of frequency (3.1 to 10.6 GHz). This higher power gain is attributed to FBB and inductive peaking approaches. Fig. 10 illustrates the pre/post layout simulation results of LNA1 circuit. Fig. 11 compares post-layout and pre-layout simulation results of NF. It has a minimum post-layout NF of 3.9 dB. It is achieved by this low power LNA1 due to the optimized interstage matching. This LNA1 gain is improved by the presence of non-zero bulk-transconductance, which does not result in excessive power consumption. To achieve forward biasing, the bulk potential is adjusted to have zero passing current in the MOS body. To guarantee lower unwanted losses and prevent DC power consumption (flow of current) in transistor body, a series resistive ($R_b$) current blocking is used. The post-layout simulation results of NF in high frequency had little deviations due to low power design but we still have good performance considering power gain and NF over a frequency range of 3.1-10.6 GHz. Shunt peaking has been employed in high frequency for gain improvement, however the parasitic components associated with $L_{d1}$ and $L_{d2}$ degraded the NF.

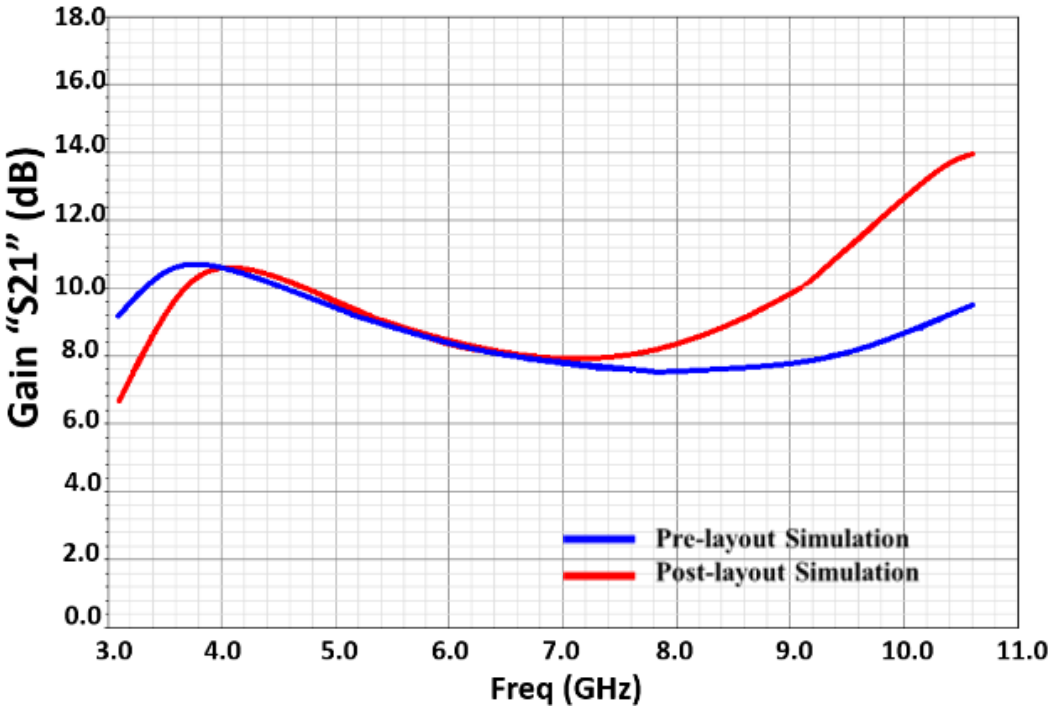


Fig. 10. Gain (S21) pre- and post-layout simulation results of LNA1

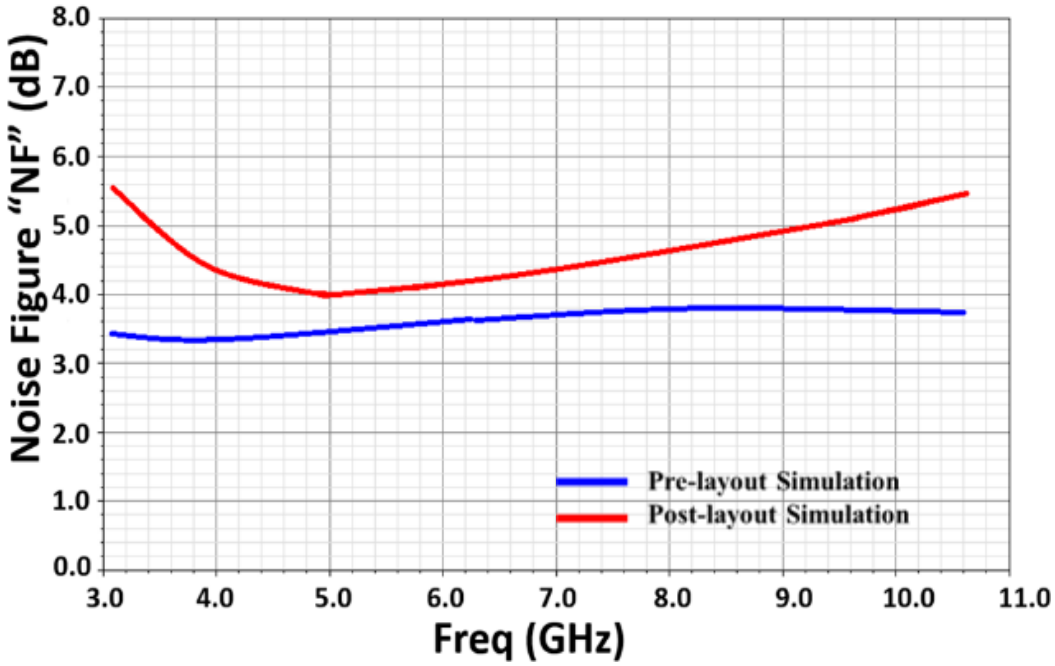


Fig. 11. Noise Figure pre- and post-layout simulation results of LNA1

### 4.1.2.LNA2 Gain and NF

The proposed design LNA2 has a 13.3±0.3 dB gain over the ultra-wideband frequency range (3.1-10.6) GHz. The advantage of using FBB and gate peaking techniques reflects the highly flattened and boosted power gain. Fig. 12 shows the power gain simulation results of LNA2. Fig. 13 previews noise figure simulation results of LNA2. As shown in Fig.13, LNA2 with current reuse CS-CS configuration has a minimum NF of a 3.14 dB (post-extraction).

## 4.2. Input and Output Impedance Matching

### 4.2.1.LNA1 Input and Output Impedance Matching

The low input return loss of the LNA1 is obtained through the utilization of an input CG stage with source degeneration technique, which results in the implementation of high impedance inductive path ($L_{S1}$). As illustrated in Fig. 14, the $S_{11}$ factor is less than -10 dB for the required frequency range (3.7~10.6 GHz). In Fig. 14, due to parasitic the post layout simulation results differ from pre-layout simulation results. This is due to the source degeneration blocking path ($L_{s1}$) and input path parasitic components of ($C_{gs1}$ and $L_{g1}$). This is also indicated by the additional high quality factor resonance of ($C_{gs1}$ and $L_{g1}$) at 4.6 GHz. With the use of the high resistive termination ($R_{out}$) and the gain shunt peaking circuit, output impedance matching is controlled. $S_{22}$ factor is less than -6.0 over the defined frequency range, as seen in Fig. 15.

### 4.2.2.LNA2 Input and Output Impedance Matching

The wideband good input impedance matching of LNA2 is utilized by using source degeneration technique with inductor $L_{s1}$. In addition, the feedback of the input stage with shunt resistive-capacitive combination plays an important role in widening the input matching of the designed LNA2 and reducing the quality factor of the input matching circuit in the LNA2. As shown in Fig.16, the input impedance matching ($S_{11}$) is less than -7 dB over the defined frequency range. In addition, the pre-layout simulation and post-layout results are shown by Fig.16. $S_{22}$ factor of LNA2 is less than -7.5 dB as illustrated in Fig.17. Thanks to the shunt peaking mechanism to have good output return loss of LNA2 circuit which is matched to fifty ohms of the next stage in the RF receiver chain.

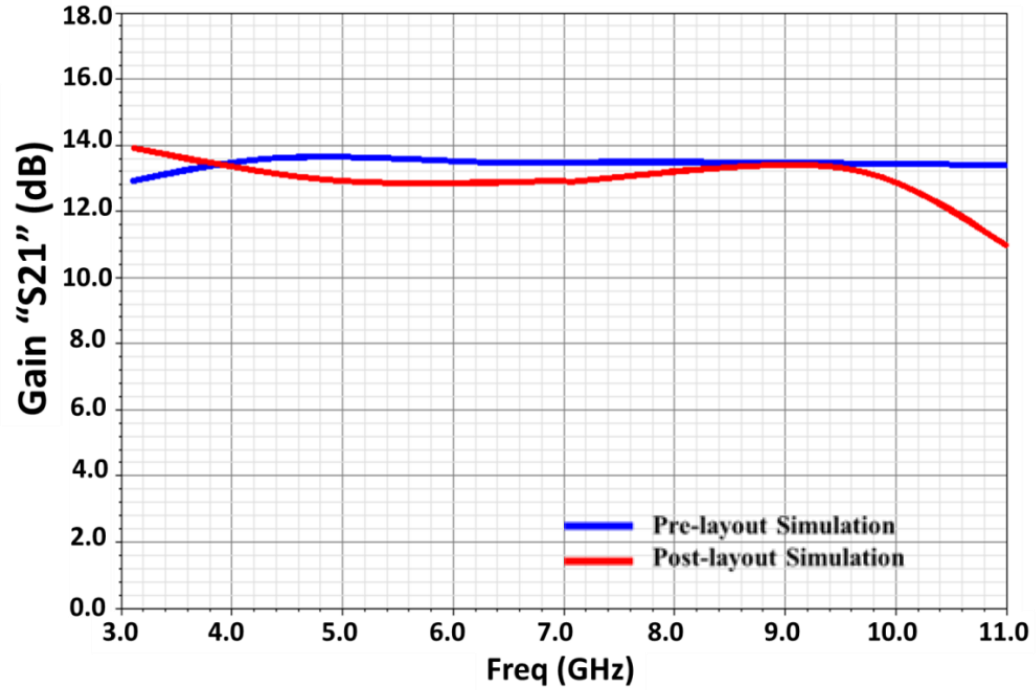


Fig. 12. Gain (S21) pre- and post-layout simulation results of LNA2

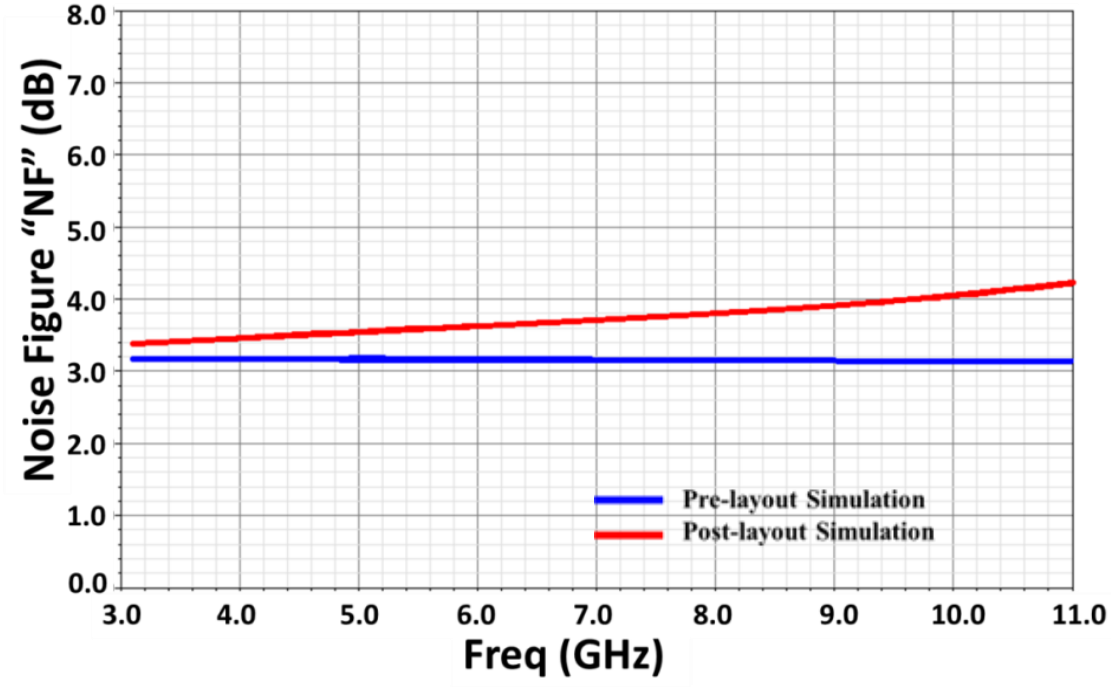


Fig. 13. Noise Figure pre- and post-layout simulation results of LNA2

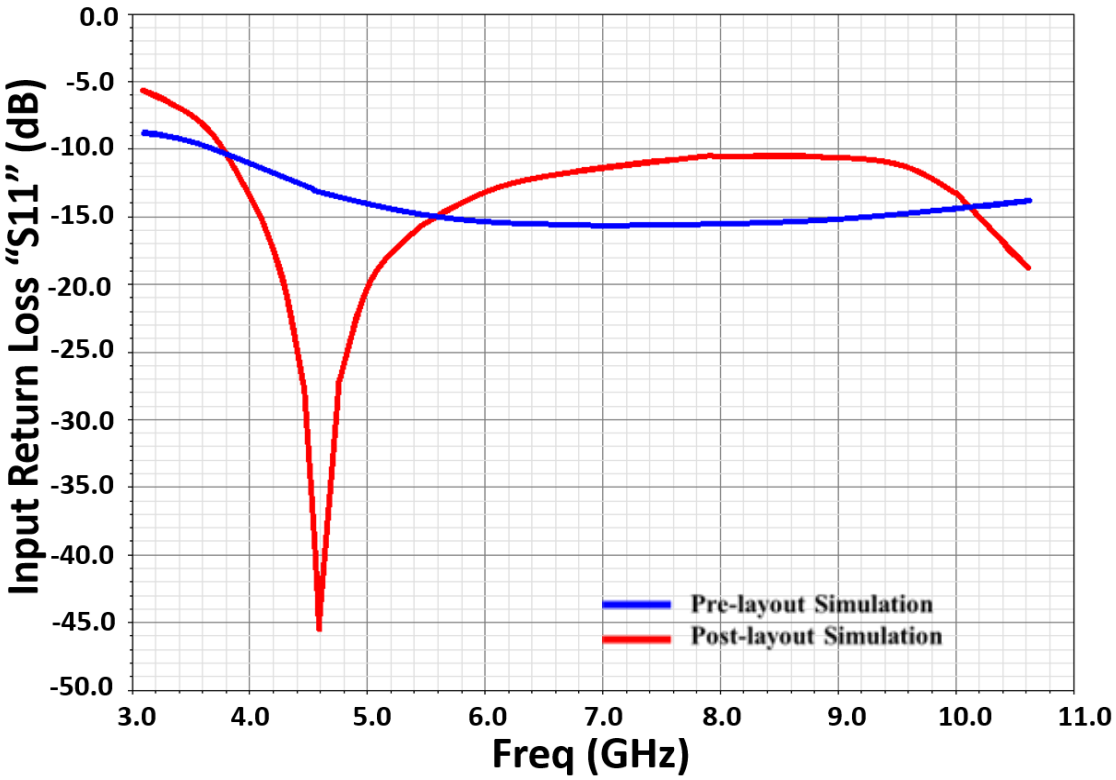


Fig. 14. Input impedance matching pre- and post-layout simulation results of LNA1

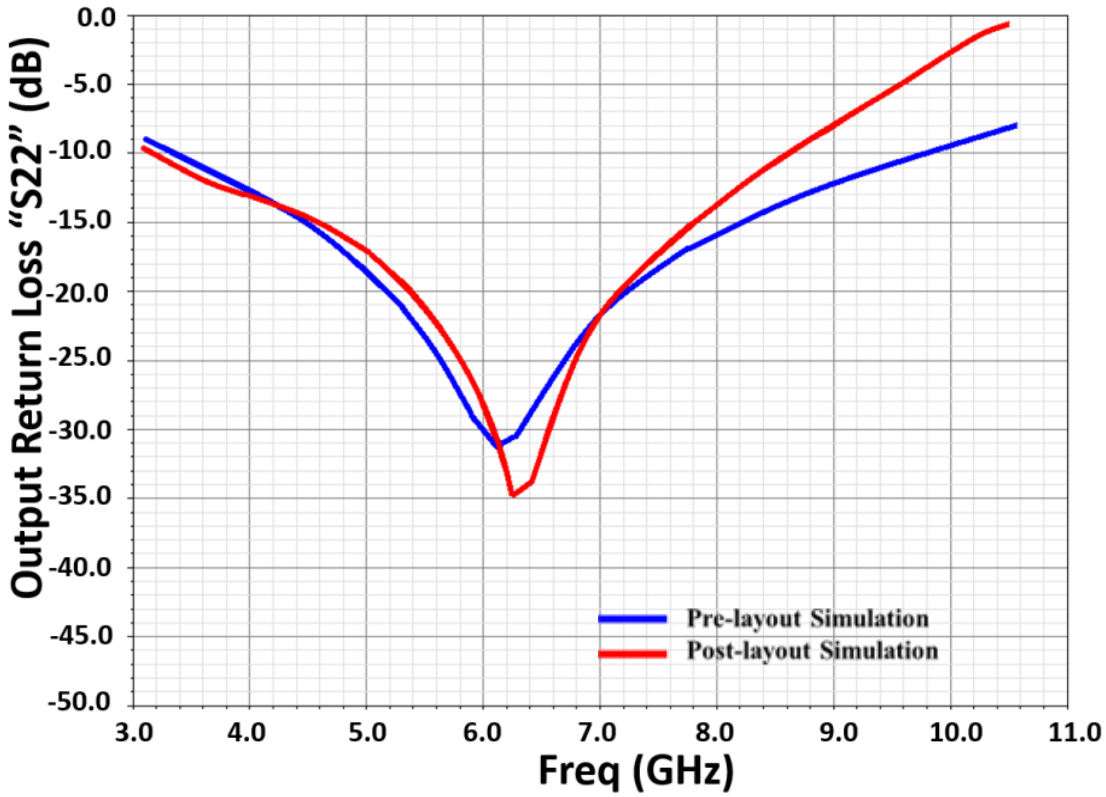


Fig. 15. Output impedance matching pre- and post-layout simulation results of LNA1

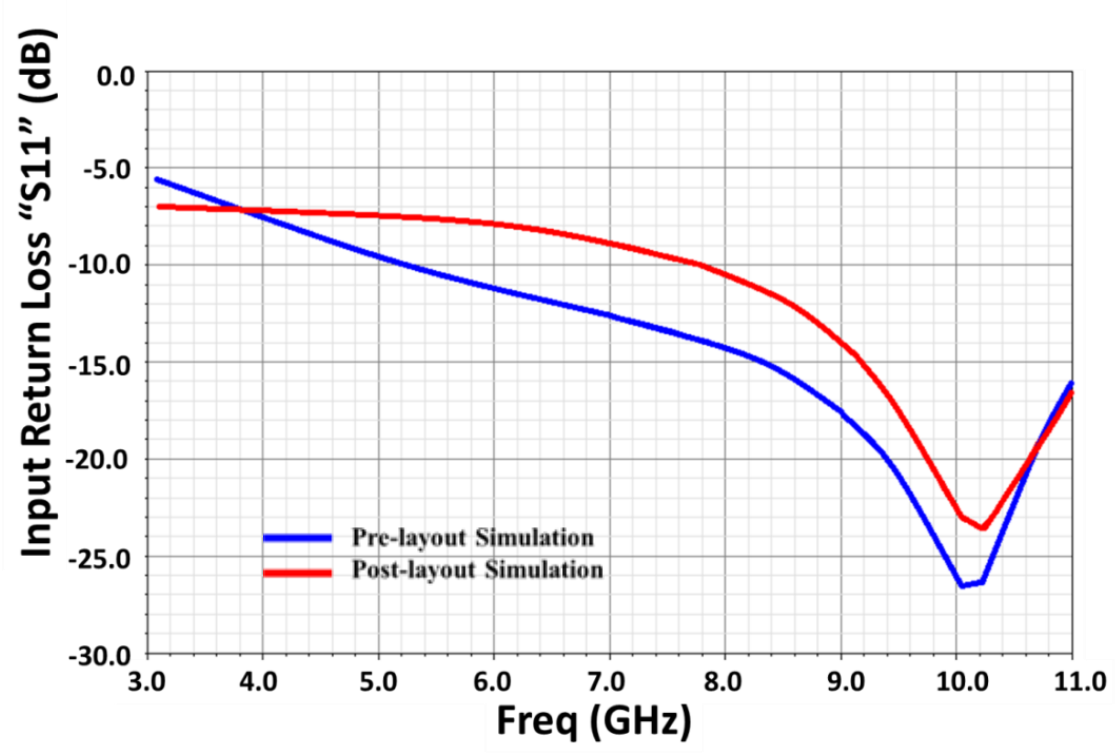


Fig. 16. Input impedance matching pre- and post-layout simulation results of LNA2

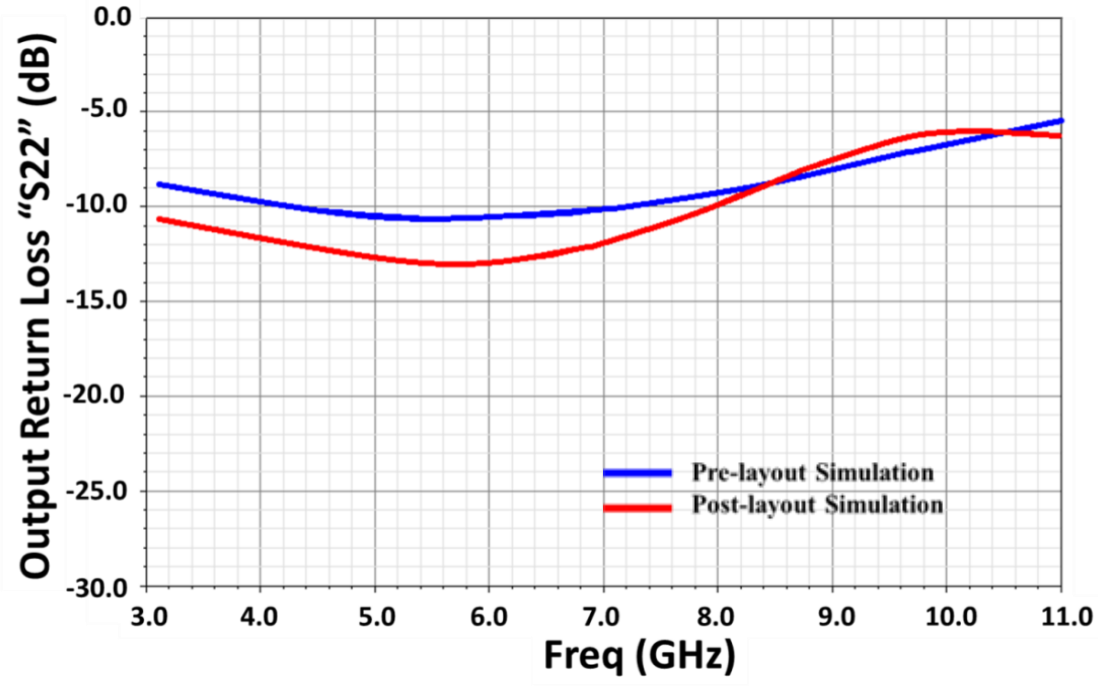


Fig. 17. Output Impedance matching pre- and post-layout simulation results of LNA2

### 4.3 Stability, Linearity and DC Power Consumption

The proposed LNAs are unconditionally stable over the desired range of frequency (UWB 3.1 ~10.6 GHz). LNA1 dissipates only 1.09mW from a 0.65V power source. In addition, 1-dB compression point $P_{1dB}$ is -14.58 dB. LNA1 has a -8.1 dBm input third intercept point (*IIP3*) obtained at mid-band of its desired frequency spectrum. LNA2 drives 10.7 mA from a voltage source with 0.615V with a dissipated power of 6.58 mW. Over the UWB frequency range, 1-dB compression point $P_{1dB}$ is -15.8 dB, and the input third intercept point (*IIP3*) of LNA2 is -9.4 dBm. These indicate the linear performance of the proposed LNAs. Table 3 and Table 4 obtain the LNAs performance with different process corners, temperatures and voltages.

**Table 3:** LNA1 Performance with Different Process corners, Temperatures and Voltages

| LNA1* | Performance | $V_{DD}$= 0.585 V | | | $V_{DD}$= 0.65 V | | | $V_{DD}$ = 0.715 V | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 20 ºC | 27 ºC | 50 ºC | 20 ºC | 27 ºC | 50 ºC | 20 ºC | 27 ºC | 50 ºC |
| tt | Gain (dB) | 11.01 | 10.95 | 10.73 | 12.52 | 12.50 | 12.40 | 13.31 | 13.12 | 12.97 |
| | NF (dB) | 3.81 | 3.88 | 3.97 | 3.85 | 3.90 | 3.99 | 3.86 | 3.87 | 3.95 |
| ff | Gain (dB) | 11.10 | 11.03 | 10.94 | 12.76 | 12.70 | 12.63 | 13.28 | 13.22 | 13.12 |
| | NF (dB) | 3.69 | 3.78 | 3.89 | 3.82 | 3.83 | 3.89 | 3.83 | 3.84 | 3.89 |
| fnsp | Gain (dB) | 10.93 | 10.84 | 10.73 | 12.49 | 12.40 | 12.34 | 13.14 | 13.07 | 13.00 |
| | NF (dB) | 3.84 | 3.89 | 4.03 | 3.81 | 3.87 | 3.94 | 3.90 | 3.92 | 3.99 |
| snfp | Gain (dB) | 10.91 | 10.83 | 10.72 | 12.45 | 12.38 | 12.02 | 13.13 | 13.09 | 12.99 |
| | NF (dB) | 3.84 | 3.88 | 3.98 | 3.80 | 3.88 | 4.08 | 3.89 | 3.91 | 4.01 |
| ss | Gain (dB) | 10.84 | 10.72 | 10.68 | 12.15 | 12.10 | 11.87 | 13.04 | 13.01 | 12.92 |
| | NF (dB) | 3.82 | 3.8 | 4.02 | 3.94 | 4.00 | 4.12 | 3.90 | 3.98 | 4.13 |

*maximum gain and minimum NF are reported.

**Table 4:** LNA2 Performance with Different Process Corners, Temperatures and Voltages

| LNA2* | Performance | $V_{DD}$= 0.554 V | | | $V_{DD}$= 0.615 V | | | $V_{DD}$ = 0.677 V | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 20 ºC | 27 ºC | 50 ºC | 20 ºC | 27 ºC | 50 ºC | 20 ºC | 27 ºC | 50 ºC |
| tt | Gain (dB) | 12.56 | 12.44 | 12.29 | 13.99 | 13.90 | 13.86 | 14.13 | 14.05 | 13.99 |
| | NF (dB) | 2.84 | 2.89 | 2.97 | 3.14 | 3.19 | 3.22 | 3.18 | 3.29 | 3.36 |
| ff | Gain (dB) | 12.59 | 12.48 | 12.35 | 14.02 | 13.96 | 13.88 | 14.16 | 14.12 | 14.06 |
| | NF (dB) | 2.79 | 2.81 | 2.90 | 3.10 | 3.10 | 3.18 | 3.19 | 3.20 | 3.29 |
| fnsp | Gain (dB) | 12.49 | 12.39 | 12.23 | 1.3.86 | 13.84 | 13.81 | 14.09 | 14.01 | 13.97 |
| | NF (dB) | 2.87 | 2.94 | 3.02 | 3.17 | 3.21 | 3.26 | 3.25 | 3.31 | 3.35 |
| snfp | Gain (dB) | 12.50 | 12.40 | 12.22 | 13.85 | 13.83 | 13.82 | 14.07 | 14.00 | 13.97 |
| | NF (dB) | 2.88 | 2.93 | 3.02 | 3.18 | 3.22 | 3.27 | 3.24 | 3.30 | 3.36 |
| ss | Gain (dB) | 12.40 | 12.32 | 12.14 | 13.80 | 13.79 | 13.76 | 14.02 | 13.96 | 13.91 |
| | NF (dB) | 2.95 | 2.99 | 3.09 | 3.21 | 3.29 | 3.31 | 3.29 | 3.38 | 3.41 |

*maximum gain and minimum NF are reported.

The performance of the presented LNAs in comparison to the recently published UWB LNAs is summarized in Table 5. It demonstrates that, in comparison to its peers, the proposed LNAs attain comparable and competitive FoMs.

**Table 5**: Ultra-wideband low noise amplifiers performance summery in comparison to recently published low power UWB LNAs

| **Reference** | **This Work*** | | **[5]*** | **[6]** | **[7]*** | **[8]*** | **[9]** | **[10]** | **[11]*** |
|---|---|---|---|---|---|---|---|---|---|
| | **LNA1** | **LNA2** | | | | | | | |
| **CMOS Process** | **130 nm** | **130nm** | 90nm | 180nm | 130nm | 65nm | 130nm | 180nm | 180nm |
| **BW (GHz)** | **3.1-10.6** | **3.1-10.6** | 34.2-37.8 | 20-28 | 7-18 | 2.1-13.2 | 3.1-10.6 | 3.1-10.6 | 3.1-10.6 |
| **Max. Gain (dB)** | **12.5** | **13.9** | 19.1 | 14 | 22.5 | 15 | 19 | 12.55 | 14 |
| **Min. NF (dB)** | **3.9** | **3.19** | 4.2 | 4.6 | 2.29 | 5.5 | 4.3 | 3.95 | 3 |
| **S11 (dB)** | **< -10** | **< -7** | ---- | <-10 | <-9.6 | < -10 | <-12 | < -10.5 | < -10 |
| **S22 (dB)** | **< -6** | **< -7.5** | ---- | <-10 | ---- | < -10 | <-10 | < -15.9 | < -4 |
| **PD (mW)** | **1.09** | **6.58** | 1.4 | 12 | 45.15 | 2.9 | 4.65 | 5.2 | 2 |
| **FoM1** | **22.05** | **4.94** | 11.69 | 2.02 | 2.39 | 10.43 | 6.8 | 6.47 | 17.5 |
| **FoM2** | **59.12** | **14.94** | 30.12 | 4.95 | 7.89 | 22.53 | 18.12 | 12.5 | 54 |

$FoM_1 = (Gain \times BW)/(NF \times P_D)$, $FoM_2 = (Gain \times BW)/((F-1) \times P_D)$, NF= *10 log (F-1)* *post-layout simulation results

## 5. Conclusions

In this paper, two low power wideband LNAs utilizing current reuse with FBB technique are presented. LNA1 is an ultra-low power CMOS UWB LNA with enhanced power gain

and minimized noise figure over the UWB frequency range utilizing the forward body-biasing technique. CG and CS stages are used for LNA implementation; in a current reuse arrangement, they are terminated by a shunt resistive load. With the help of gain shunt peaking and forward body biasing, LNA1 achieves significant FoMs while dissipating only 1.1 mW of power. LNA2 uses current reuse CS-CS topology. LNA2 achieves a high post-layout gain of 13.6dB. It has a flatten post-layout noise figure with a minimum of 3.19 dB through the UWB spectrum of frequency. It dissipates only 6.58 mW of power from a 0.615V power supply. Both LNAs have good isolation performance. LNA1 and LNA2 have output and input matching impedance over the ultra-wideband (UWB) frequency range of interest (3.1~10.6 GHz).

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# عن استخدام تقنية الانحياز الأمامي لقاعدة الترانزستور في تصميم وتنفيذ المكبرات منخفضة القدرة واسعة النطاق الترددي منخفضة الضوضاء

## الملخص

يقدم هذا البحث منهجية جديدة لتصميم وبناء المكبرات منخفضة الضوضاء متسعة النطاق الترددي ذات استهلاك قدرة منخفض. يتم ذلك عن طريق توظيف تقنية الانحياز الأمامي للقاعدة في ترانزستور تكنولوجيا معدن - عازل - شبه موصل المتكاملة. تم من خلال هذا البحث تقديم تصميمين مختلفين من المكبرات منخفضة الضوضاء واسعة النطاق الترددي والتي تم تخفيض القدرة المستهلكة بها عن طريق التصميم بمساعدة تقنية الانحياز الأمامي لقاعدة بوابة الدخل الأساسية للمكبر. التصميمين المقدمين تم تصميمهما بتوصيل دائرة المكبر ليتم إعادة استخدام التيار المستمر لتوفير القدرة لما لهذه الدائرة من خصائص جيدة مع توفيرها للطاقة المستهلكة داخل تلك المكبرات. بمساعدة إعادة استخدام التيار الكهربي المستمر مع تقنية الانحياز الأمامي لقاعدة الترانزستور والتي تزيد وتضيف إلى الموصلية الانتقالية للترانزستور. تبدو تقنية الانحياز الأمامي للقاعدة وكأن الترانزستور يحتوي على بوابة أخرى إضافية ومن خلال ذلك نستطيع الوصول لمعدلات كسب كبيرة بالإضافة إلى معاملات ضوضاء منخفضة مع استهلاك قدرة منخفض جدا. يظهر تأثير وفاعلية التصميمات المقدمة باستخدام التقنيات المقترحة في تميز وتحسن معاملات أداء المكبرين المقدمين من خلال هذا البحث. فالمكبر الاول له معاملات ضوضاء تصل إلى أقل من ٣,٩ ديسيبل ويصل معامل كسب القدرة لهذا المكبر إلى ١٢,٥ ديسبل بينما يستهلك ١ ميللي وات فقط من القدرة. أما المكبر الثاني فله معامل كسب قدرة يصل إلى ١٣,٦ ديسبل بينما معاملات الضوضاء له فهي أقل من ٣,١٩ ديسبل بينما يستهلك ٦,٥ ميللي وات من القدرة اللحظية. وقد تم تصميم واختبار ومحاكاة هذه المكبرات منخفضة القدرة منخفضة الضوضاء واسعة النطاق الترددي باستخدام تكنولوجيا -معدن- عازل - شبه موصل المتكاملة.