Journal of
Engineering Sciences
Faculty of Engineering
Assiut University
JES
مجلة
العلوم الهندسية
كلية الهندسة
جامعة أسيوط
journal homepage: http://jesaun.journals.ekb.eg

Optimized Inexact adder for Approximate Computing Applications

Received 6 March 2025; Revised 16 September 2025; Accepted 17 September 2025

Narmadha G[1]
Deivasigamani S[2]
P. Pugazhendiran[3]
Jeya Prakash K[4]
Prakash P[5]

Keywords
Area, Power consumption, Approximate Adder, Image

Abstract: For appropriate multimedia devices, power consumption should be less and it plays a major role in designing such devices. Image compression methods make use of a variety of signal processing architectures and algorithms. In many multimedia applications, people can extract useful information from slightly inaccurate outputs. As a result, producing precise results is not essential. Adders are an essential arithmetic module in digital signal processing platforms which help to regulate the system's power and area utilisation. The detrimental development and use of approximation adders have been based on trade-off characteristics including time, area and power consumption, as well as the fault tolerance condition in some applications. This article analyses the area, latency, and power consumption of different kinds of approximate adders and existing adders. Additionally, a high-speed, power-efficient and approximate adder is developed which outperforms the current adders in terms of performance. The proposed adder can be used in arithmetic modules of several computing systems including image processing, data mining and cryptographic applications in which the exact outputs are not necessary. The proposed and existing approximate adders are synthesized by using Xilinx and the Microwind is used to measure the power consumption.

1. Introduction

An increasingly popular method for developing high-performance, energy-efficient computing algorithms is approximate (inexact) computing. A ripple carry adder is one example of an arithmetic circuit which utilises the significant use of approximate computation. When certain combinations of inputs are used, approximate adders produce inaccurate results for both carry and sum. Thus, the system's hardware requirements for imprecise computation are decreased. Consequently, the system achieves fast speed and low power consumption through approximation computation. Approximate computing is a good option, though, for Digital Signal Processor applications where precise results are not

[1] Associate professor, Dept. of EEE, Sethu Institute of Technology, India. gnarmadhame@gmail.com
[2] Asst. Professor, Faculty of Engineering, Technology, & Built Environment, UCSI University, Kuala Lumpur, Malaysia
3 Professor, Dept. of EEE, IFET College of Engineering, Villupuram, India.
4 Dept. of ECE, Kalasalingam Academy of Research and Education, Virudhunagar, India.
5 Asst. Professor, Dept. of EEE, K. Ramakrishna College of Technology, India.

https://doi.org/10.21608/jesaun.2025.366117.1440
This is an open access article under the CC BY-NC-ND license (http://creativecommons.org/licenses/by-nc-nd/4.0/).

necessary, such as image, audio, and video processing. The inexact adders are analyzed based on the various parameters to get an optimized design for different applications [1] where the accurate results are not necessary without compromising the design performance. The design complexity and power dissipation are also reduced with the efficient use of approximate design structures. Adder structures can be implemented with the many digital Technologies [2] like Complementary Pass Transistor Logic (CPL), Transmission Gate Adder (TGA) and Double Pass Transistor Logic (DPL) for reducing the Power dissipation of the digital design. The design accuracy is improved by reducing the tradeoff parameters like power and area consumption with the use of [3] High Performance Error Tolerant Adders and Multiplexer

based arithmetic full adders (MBAFA). A wide range of approximation adder structures [4 – 7] are presented, and its performance is evaluated according to the area, power, accuracy and speed of the design. Equal segmentation Adder (ESA) is designed in [8], but results in lowest degree of accuracy. The inexact full adders are analyzed based on the power and area consumption [9]. Accuracy is achieved by masking the carry propagation at run time [10], and the estimated adder is based on the carry look ahead adder. It is utilized for error-tolerant applications and reduces both power and delay. In multimedia signal processing and data mining, approximate adder structures are utilized because they are error-tolerant and do not require accurate computation. In 4-2 compressor tree [11], area consumption is reduced by replacing Ex–or gate by OR gate. In most of the image processing applications, inexact multipliers [12] which are built with approximate adders are used. Soft DSP employs [13] algorithmic noise tolerant (ANT) error management techniques to make up for algorithmic performance reduction caused by input-dependent defects. A prediction-based error management technique was put forth to enhance the filtering algorithm's efficiency even in cases of the occurrence of error due to inexact computation. Inexact computing is also used in DCT based image compression techniques [14 & 15] in which the design parameters such as delay, PSNR and energy are analyzed. The area consumption is also reduced in the accurate adders [16, 17] by optimizing the circuit design. The optimized approximate adder is designed [18, 19] with the reduced power, area and delay only by using one Exor and one OR gate. The existing inexact adder designs are explained in Section 2. The proposed adder design is depicted in Section 3. The performance of proposed and existing approximate designs is analyzed in Section 4. Section 5 depicts the conclusion of the paper.

2. Existing Inexact Adders

Different existing inexact adders are taken in to account for analyzing the performance of proposed adder. The optimized adder which yields high performance [19] is considered as approximate 1. The adders proposed in [3], MBAFA1 and MBAFA2 are considered as approximate 2 and 3 respectively. The CNFET based adder which is proposed to reduce

power consumption [4] is taken as approximate 4. In [5] various approximate adders are designed and analyzed to reduce the chip dimension and are taken as approximate 5, 6 and 7. The XOR and XNOR based adders are proposed in [6] to reduce the number of transistors and power consumption and are referred as approximate 8, 9 and 10. The number of transistors count is reduced by replacing the xor gate by or gate in approximate adder [12] and it is considered as approximate 11. High speed error tolerant adder [15] which is used in image processing applications is referred as approximate 12.

3. Proposed Inexact Adder

The Proposed Inexact adder is designed by using only one OR gate and one NAND gate. Whereas, the accurate adder consists of two XOR gates, three AND gates and one OR gate. Compared to the existing accurate adder, the proposed adder consists of only two gates. So, the number of transistors, chip size and power consumption is reduced automatically. The proposed design is shown in the Fig. 1. The sum and carry equations are given below.

$$SUM = ((B + C) . A)'$$
$$CARRY = A$$

The SUM and CARRY values of the proposed structure and existing structures are given in Table 1.

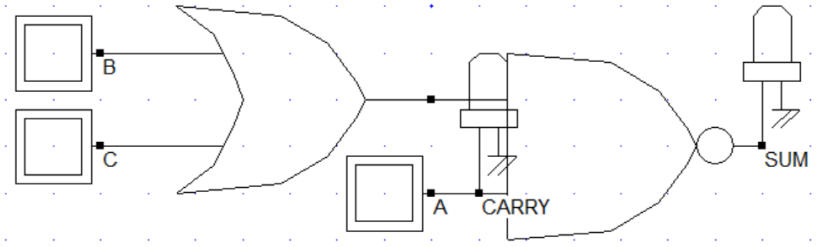

Fig. 1. Proposed Inexact Adder

4. Performance Analysis

The proposed and existing inexact adders are simulated with the use of Microwind 3.0. The design trade off parameters such as chip frequency, chip dimension, number of required CMOS transistors and Power consumption are measured and its values are shown in Table 3. From the above simulated outputs, it is clear that the suggested inexact adder executes better while considering the tradeoff parameters. The power consumption is considerably reduced with the increase in chip frequency and are given in Fig. 2 and 3 respectively. From the Table 3, the Mean Error Distance (MED) is calculated as 3 Normalized Mean Error Distance (NMED) is 0.4135. It can be implemented where nano-scale high-speed multiplier [20] has to be designed. The various digital designs are used in architecture [21] also.

Table 1. Output values of accurate adder & approximate adders 1 to 7

Inputs			Outputs															
			Accurate		App. 1		App. 2		App. 3		App. 4		App. 5		App. 6		App. 7	
A	B	C	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
0	0	1	1	0	1	0	1	0	1	0	1	0	1	1	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	1	1	0	1	0	1	0	0	1	0	1	1	1	0	1
1	0	0	1	0	1	1	0	1	1	0	1	0	1	0	1	0	1	0
1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	1	1	0	1
1	1	0	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1

Table 2. Output values of approximate adders 8 to 12 & proposed adder

Inputs			Outputs											
			App. 8		App. 9		App. 10		App. 11		App. 12		Proposed	
A	B	C	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
0	0	1	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	0	0	0	1	0	1	0	1	0
0	1	1	1	0	0	1	0	1	0	1	0	0	1	0
1	0	0	0	1	0	0	0	0	1	0	1	1	1	1
1	0	1	1	0	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	1	1	0	1	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1	0	1	1	1	0	1

Table 3. Simulation Outputs of Proposed and Existing Inexact Adders

Adder	Chip Dimension (Width X Height) (µm)	Chip Frequency in (GHz)	Number of transistors	Consumption of Power (nW)	Total Error Distance	Error Rate (%)
App. 1	7 X 10	0.965	12	1.832	4	25
App. 2	13 X 12	0.167	18	4.095	4	25
App. 3	14 X 12	0.25	20	3.559	4	25
App. 4	15 X 11	0.25	32	7.057	2	12.5
App. 5	8 X 10	0.25	12	4.052	2	12.5

Adder	Chip Dimension (Width X Height) (µm)	Chip Frequency in (GHz)	Number of transistors	Consumption of Power (nW)	Total Error Distance	Error Rate (%)
App. 6	17 X 12	0.25	38	6.824	2	12.5
App. 7	19 X 12	0.25	46	7.762	2	12.5
App. 8	11 X 11	0.333	22	5.11	8	50
App. 9	15 X 12	0.25	30	5.26	4	25
App. 10	17 X 12	0.25	36	5.424	2	12.5
App. 11	10 X 10	0.25	18	3.297	2	12.5
App. 12	8 X 10	0.25	12	8.663	2	12.5
Proposed	6 X 11	1.17	10	0.965	5	31.25

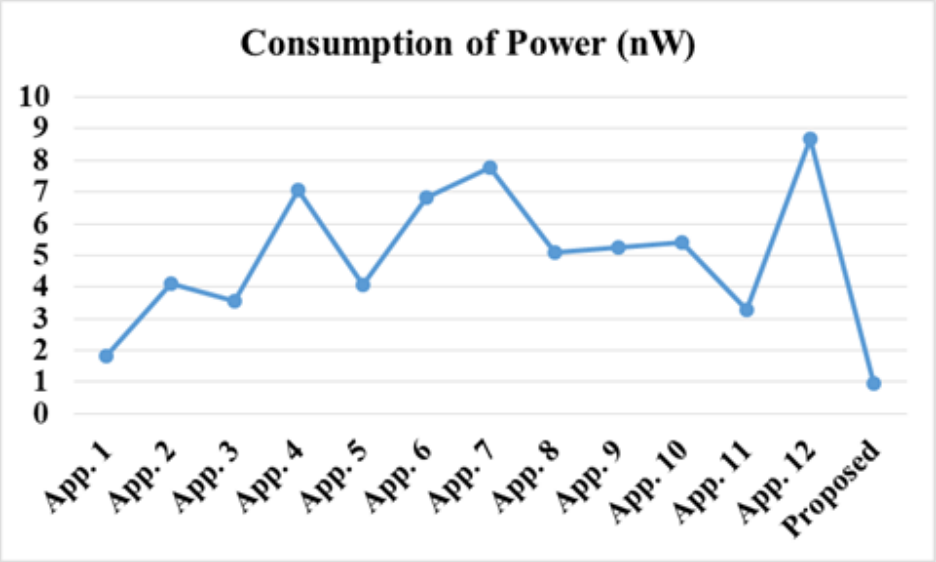

Fig. 2. Simulated Output for Consumption of Power (nW)

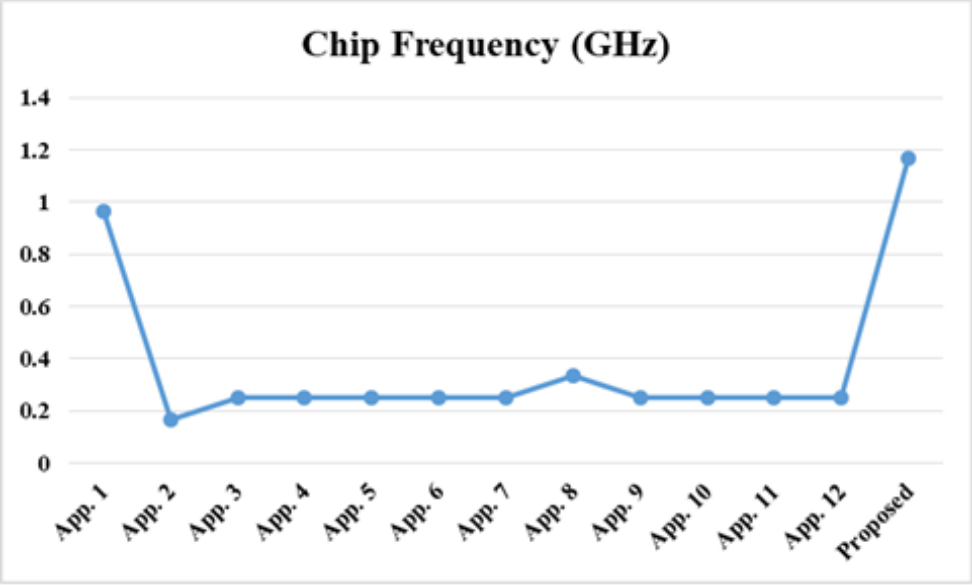

Fig. 3. Simulated Output for Chip Frequency (GHz)

5. Conclusions

This work reveals the overall performance of existing and proposed inexact adders. After analysing the performance, it is concluded that the proposed inexact adder has high chip frequency chip dimension and low power consumption while comparing to the existing inexact adders. Because of the high speed and low power consumption, the suggested inexact adder can be recommended for the applications where the approximate computing is implemented especially for image processing applications and it can be implemented by using FPGA.

References

[1]. Junqi Huang , Nandha Kumar Thulasiraman , Haider Almurib , et al. "Analysis of Approximate adders with single functional error", *TechRxiv.* January 02, 2024.

[2]. Ashim Gogoi, Vinay Kumar, "Design of Low Power, Area Efficient and High-Speed Approximate Adders for Inexact Computing", IEEE International Conference on Signal Processing and Communication , Page(s):452 – 456, 2016

[3]. R. Jothin & C. Vasanthanayaki, "High Performance Error Tolerant Adders for Image Processing Applications", IETE Journal of Research, IETE Journal of Research, DOI: 10.1080/03772063.2018.1535920, pp.1- 12, 2018

[4]. Fazel Sharifi, Atiyeh Panahi, Mohammad Hossein Moaiyeri, Hojjat Sharifi & Keivan Navi, "High Performance CNFET-based Ternary Full Adders", IETE Journal of Research, IETE Journal of Research, DOI:10.1080/03772063.2017.1338973, pp. 1- 8, 2017.

[5]. Jeevan Jot Singh, Dr. Jyoti Kedia, "A Comparative Analysis of Different Approximate Adders Used for Image Compression and Image Addition", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Volume 7, Issue 1,pp. 39 – 44 , 2018.

[6]. Zhixi Yang, Ajaypat Jain, Jinghang Liang, Jie Han and Fabrizio Lombardi, "Approximate XOR/XNOR-based Adders for Inexact Computing", Proceedings of the 13th IEEE International Conference on Nanotechnology Beijing, China, pp. 690 -693., 2013.

[7]. Vaibhav Gupta, Debabrata Mohapatra, Anand Raghunathan, and Kaushik Roy, "Low-Power Digital Signal Processing Using Approximate Adders, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 32, No. 1, pp.124 – 137, 2013.

[8]. Honglan Jiang, Jie Han, Fabrizio Lombardi, "A Comparative Review and Evaluation of Approximate Adders", Proceedings of the 25th edition on Great Lakes Symposium on VLSI, pp. 343-348, 2015.

[9]. Sunil Dutt, Sukumar Nandi, and Gaurav Trivedi, "Analysis and Design of Adders for Approximate Computing", ACM Trans. Embed. Comput. Syst. 17, 2, Article 40 , 28 pages, December 2017.

[10]. Tongxin Yang, Tomoaki Ukezono, Toshinori Sato, "A Low-Power Yet High-Speed Configurable Adder for Approximate Computing", IEEE International Symposium on Circuits and Systems (ISCAS), 2018.

[11]. J.Anjana, K.Shanthalakshmi, "Design of Adders and 4-2 Compressors for Approximate Multipliers", International Journal of Innovative Research in Science, Engineering and Technology, Volume 7, Special Issue 1, pp. 12 -18, 2018.

[12]. Kalvala Srikanth, "Design of Low Power and Area Efficient Approximate Multipliers" International Journal of Advanced Research Trends in Engineering and Technology, Vol. 4, Issue 3, pp. 252 – 260, 2017.

[13]. Rajamohana Hegde, Naresh R. Shanbhag, "Soft Digital Signal Processing", IEEE Transactions on Very Large-Scale Integration (VLSI) systems, Vol. 9, No. 6, pp. 813 -823, 2001.

[14]. Haider A.F.Almurib, T. Nandha Kumar and Fabrizio Lombardi, "Approximate DCT Image Compression using Inexact Computing", IEEE Transactions on Computers, Volume: 67, Issue: 2 , pp. 149 – 159, 2018.

[15].S Geetha and P Amritvalli, "High speed error tolerant adder for multimedia applications", J. Electron. Test., Vol. 33, no. 5, pp. 675–688, 2017.

[16]. G.Narmadha, Dr. K. Balasubadra, S. Deivasigamani, "Design and Implementation of Time Efficient Carry Select Adder using FPGA", International Journal of Applied Engineering Research, Volume 10, Number 3, pp. 7215-7227, 2015.

[17]. G. Narmadha, Dr. K. Balasubadra, "An Optimized Montgomery Multiplier for Public Key Cryptography", International Journal of Advanced Engineering Technology, Vol. VII, Issue I, pp. 05 – 07, 2016.

[18]. Manickam Ramasamy, G. Narmadha, S. Deivasigamani, "Carry based approximate full adder for low power approximate computing", in Proceedings of IEEE 7th International Conference on Smart Computing & Communications (ICSCC), 2019.

[19]. Dr. G. Narmadha, Dr. S. Deivasigamani, Dr. K. Balasubadra and Mr.M.Selvaraj, "A low power and high-speed approximate adder for image processing applications", Journal of Engg. Research Vol.10 No. (1A) pp. 150-160, 2022.

[20]. SS Ahmadpour, NJ Navimipour, NU Ain, F Keresteciogl u, S Yalcin, "Design and implementation of a nano-scale high-speed multiplier for signal processing applications", Nano Communication Networks, Vol.41 No.2., 2024

[21].Ahmed Saleh Abdel Fattah, "Modern Technical Applications for Digital Design in Architecture", Journal of Engineering Sciences, Vol.45, No.2, pp.176 – 199, 2017.